An 8-GSa/s 8-bit ADC System

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Abstract

We report on an analog to digital converter (ADC) system with 8 bit resolution and a sample rate of 8 GSa/s. The system is composed of 2 thick-film hybrid substrates, each holding a silicon bipolar ADC chip and a custom CMOS memory chip.

Each ADC chip contains two differential track and hold circuits and two folding and interpolating 2 GSa/s flash digitizers. The custom memory chip accepts data at 2 GSa/s on each of two input ports, and stores the data in a 256 Kbit SRAM.

The ADC system uses time interleaving of 4 paths to reach 8 GSa/s and combines hardware dither with software calibration techniques to achieve 7.6 effective bits at low frequencies and 5.3 effective bits at 2 GHz input.

Introduction

Analog to digital converters (ADCs) with sample rates of 1 GSa/s and above have applications in digitizing oscilloscopes, waveform recorders and radar signal capture. The resolution needed for these applications is generally 6 to 8 bits.

Other ADC systems [1],[2] have reported effective bits results for sample rates of 4 GSa/s; [3] and [4] have achieved sample rates of 8 and 10 GSa/s, but with bandwidths of no more than 2 GHz. This work demonstrates a signal bandwidth of over 4 GHz and reports the highest accuracy for a real-time ADC on signal frequencies above 1 GHz.

System Overview

Fig. 1 shows the simplified block diagram of the 8-GSa/s ADC system. Two thick-film hybrid circuits are utilized; on each one there is an ADC chip and a memory chip. The 4-GSa/s ADC chip is implemented in a 25-GHz f_T silicon bipolar process for high conversion speed and accuracy. The memory is a custom CMOS SRAM implemented in a 0.6-μm CMOS process to take advantage of the high storage density of CMOS.

ADC Chip

Fig. 2 shows the block diagram of the ADC chip. An on-chip preamp provides a gain of about 7, does single-ended to differential conversion and drives the two 2-GSa/s 7-bit digitizer blocks on the chip. Signal-dependent transistor self-heating in the preamp and T/H circuits causes a 4% overshoot of the step response, which takes nearly a millisecond to fully settle out. The preamplifier generates a thermal error signal [5] on an extra pair of transistors and feeds it back into the signal path via a variable gain amplifier to cancel the thermal overshoot to about 0.25%.

The digitizer block diagram is seen in Fig. 3. Dual diode-bridge track-and-hold (T/H) circuits are used for the differential input signal, which is then passed to a differential to single-ended converter (D/S).

To speed the settling of the D/S output signal and reduce comparator power, this converter uses folding and interpolation. 66 diff pairs are grouped together using a 4-way folding circuit (see [2]) to create 18 folded outputs.

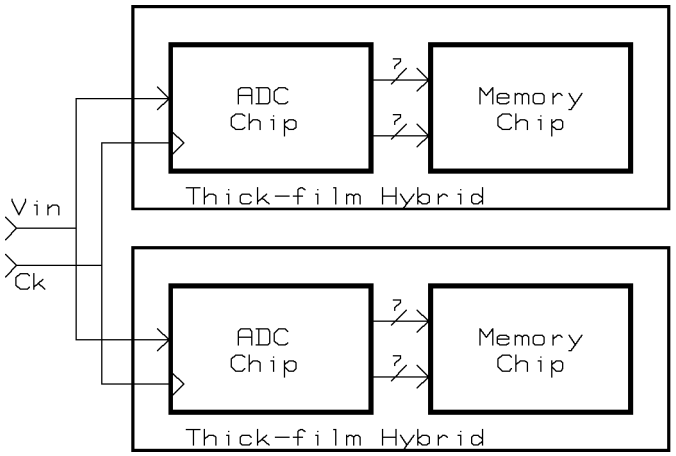

Fig. 1. Block diagram of the 8 GSa/s ADC system

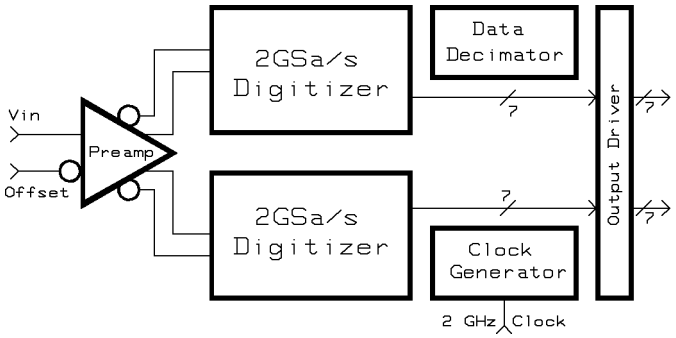

Fig. 2. Block diagram of the ADC chip

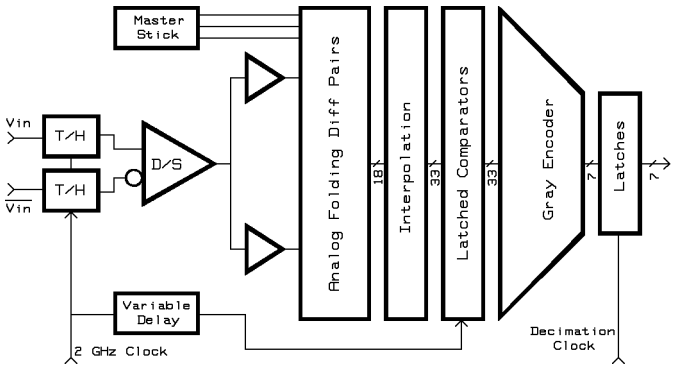

Fig. 3. Block diagram of one ADC digitizer

1:2 interpolation is used on the folded outputs to drive the 33 latched comparators. This reduces the loading on the D/S output by a factor of 2 and reduces the number of latched comparators by a factor of 4.

The latched comparator values are encoded into Gray code rather than binary. This greatly relaxes the requirements for comparator regeneration speed, because any single metastable comparator state need not be resolved before writing into memory.

Interleaving multiple ADC channels which sample signals above 2 GHz requires picosecond accuracy in timing alignment. To achieve this, on-chip variable delay circuits are included in the clock path.

TABLE I: CHIP CHARACTERISTICS

	ADC Chip	Memory Chip
Process	25-GHz f_T Si bipolar	0.6-μm CMOS
Power	12.5 W	1 W operating
Transistors	6400	1,900,000
Area	5.3 x 5.6 mm	7.1 x 8.3 mm

Packaging

Fig. 4 is a photograph of the thick-film hybrid circuit; it is 1.7 x 1.9 inches. Chip to chip bonding is used between the ADC and memory chips to keep the capacitance, and thus power, in this interface to a minimum.

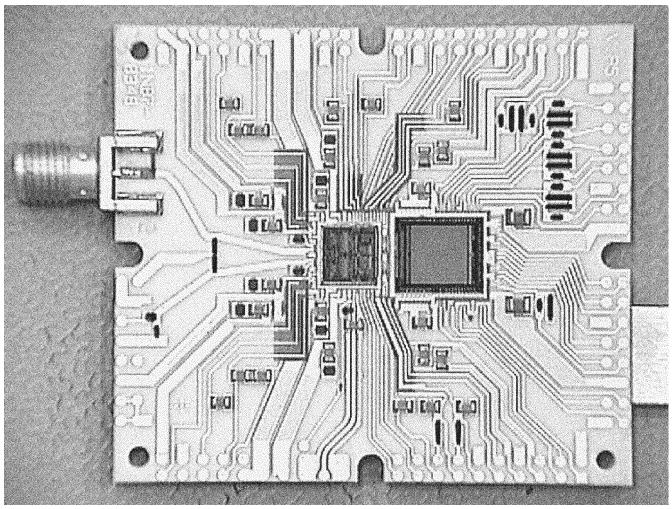

Fig. 4. Photograph of the thick-film hybrid circuit

Measurements

A. Single 2 GSa/s Digitizer Path

DNL of ± 0.3 7b LSBs was measured in the ADC chip. INL of ± 1.5 7b LSBs was measured; the INL is largely second and third harmonic distortion from the preamp, D/S and reference voltage divider. This limits the low-frequency linearity to 6.1 effective bits as seen in Fig. 5. By applying a software linearization step to the data, we can remove the static harmonic distortion to improve the low-frequency accuracy to 6.7 effective bits.

The jitter in the T/H clock was measured at 0.6 ps rms. For a 2 GHz input signal, this limits accuracy to 7 effective bits. The small-signal bandwidth of the digitizer is more than 4 GHz.

B. 8 GSa/s System

Fig. 6 shows measured effective bits versus input signal frequency for the 8 GSa/s system. The lower trace shows the effective bits achieved by simple interleaving of the linearized data from the four 2 GSa/s digitizers.

The system reaches 8-bit resolution using a 1/4 LSB offset between digitizers to provide a static dither pattern. The upper trace shows the performance after removal of this dither with a software filter. At low frequencies, the effective resolution reaches 7.6 effective bits, while at 2 GHz, the system achieves 5.3 effective bits, only 0.1 bits

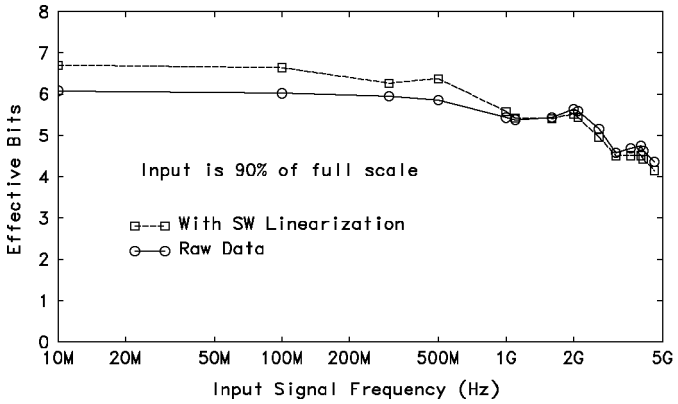

Fig. 5. Effective bits of a single 2 GSa/s path

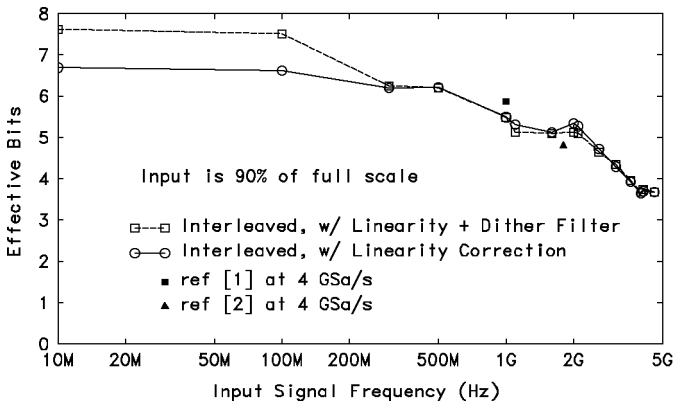

Fig. 6. Effective bits of the 8 GSa/s ADC system

worse than the accuracy of a single digitizer. Above 3 GHz, channel-to-channel mismatch dominates the errors in the 8 GSa/s system. The effective bits for the highest sub-Nyquist frequency reported for other systems are also plotted.

Conclusion

This 8 GSa/s ADC system demonstrates the world's highest reported effective bits accuracy for real-time acquisition of input signals above 1 GHz.

References

[1] Ken Rush and Pat Byrne, "A 4 GHz 8b Data Acquistion System", *IEEE Int'l Solid State Circuits Conference,* Feb 1991, pp 176-177

[2] Ken Poulton, Knud L. Knudsen, John J. Corcoran, Keh-Chung Wang, Randy Nubling, Richard Pierson, Mau-Chung F. Chang, Peter Asbeck and R.T. Huang "A 6-bit, 4 GSa/s GaAs HBT ADC", *IEEE Journal of Solid State Circuits,* Oct 1995

[3] "Four-channel, 8 GSa/s Real-time Modular Oscilloscope Mainframe" *http://www.tmo.hp.com/tmo/datasheets/English/HP54720D.html*

[4] "9362 Fast Digitizing Oscilloscope", *http://www.lecroy.com/techindex.htm*

[5] Knud L. Knudsen, US Patent 5,483,199, assigned to Hewlett-Packard Company

[C] IBM SiGe 8 GSa/s 4-bit paper??
[D] Rockwell 3 GSa/s 8-bit work??
[E] HP CMOS14 paper?
[F] HP hp25 paper?
[H] some Phillips interpolation paper?

No HP FISO paper exists

[C] a recent 8-GSa/s, 4-bit in SiGe
[?] 20 GSa/s ADC

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