

Thermal Design and Simulation of Bipolar Integrated Circuits

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Abstract

Keeping device operating temperatures within reasonable limits is necessary for reliability of all ICs, and important to achieving the expected performance for many ICs. GaAs Heterojunction Bipolar Transistors (HBTs) offer high speed and good device matching characteristics that are attractive for many high-speed circuits, but they are more susceptible than other IC technologies to the unexpected generation of very high junction temperatures. We describe the reasons for this tendency and describe an HBT S/H circuit which had device temperature rises of over 300 °C.

To address this problem we created a new thermal simulation tool called ThCalc. ThCalc calculates the temperature profile of an IC and runs fast enough to allow calculations on a whole chip. We used ThCalc to redesign the S/H IC to reduce the largest temperature rise by a factor of 2.7 with a minimal impact on circuit size.

Introduction

For all integrated circuits, keeping device temperatures within reasonable bounds is critical to long-term reliability. Most IC failure mechanisms are accelerated at higher operating temperatures; it is common to find activation energies of around 1 eV, for which an increase of 10 °C in operating temperature leads to that failure occurring in half the time. For this reason, it is usual for IC process specifications to include a maximum device junction temperature between 100 and 150 °C.

In addition, controlling device temperatures can be key to meeting performance requirements. Higher operating temperatures usually degrade device performance, for example, by reducing f_T and increasing leakage currents. Another important effect is that self-heating can cause offset and thermal “memory” effects in bipolar transistors because V_{BE} varies at -1 to -2 mV/°C. Even a temperature gradient across a chip may degrade performance by upsetting symmetry between otherwise matched devices.

Thermal effects become more pronounced when the devices run at high power densities and many recent high-speed bipolar IC processes must run at high current densities to achieve their best speeds. For example, both NTT's

25 GHz silicon process [1] [2] and the Rockwell 50 GHz GaAs HBT process [3] use current densities of up to $0.8 \text{ mA}/\mu\text{m}^2$. The silicon transistor's f_T peaks at this current density, while the GaAs HBT's f_T actually continues to rise with higher currents but the current density is limited to $0.8 \text{ mA}/\mu\text{m}^2$ for reliability reasons.

Of course, GaAs ICs suffer more from all thermal effects than comparable silicon ICs because the thermal conductivity of GaAs is only one third that of silicon. Since the thermal conductivity of semiconductors decreases at higher temperatures, this difference more than triples the operating temperatures seen in GaAs circuits for the same power and geometries. In addition, the DC current gain of GaAs HBTs is best at high current densities and with relatively short and wide emitters, both of which increase the peak device junction temperatures. In the Rockwell 50 GHz GaAs HBT process, emitter widths are $1.4 \mu\text{m}$, while the NTT silicon transistors use emitter widths of $0.35 \mu\text{m}$. For a given collector current, the $4\times$ wider HBT emitters are therefore also $4\times$ shorter; this effectively concentrates the power dissipation in a smaller linear region and increases the peak temperatures seen. For example, a small HBT device is $1.4\times 3.0 \mu\text{m}$, while the same emitter area in the silicon process will be $0.35\times 12 \mu\text{m}$. The shorter, wider transistor will have a thermal resistance $2\times$ higher solely due to geometrical considerations.

GaAs HBTs also suffer more from thermal effects than GaAs FET processes due to their high current densities. GaAs FET processes typically run at linear current densities of 0.2 to $0.5 \text{ mA}/\mu\text{m}$, while our GaAs HBT process runs at about $1.1 \text{ mA}/\mu\text{m}$.

The effect of all these factors is that for a given kind of circuit and power level, GaAs HBT circuits will tend to produce higher operating temperatures than other IC technologies. This does not mean that other technologies have no thermal problems, but simply that they are more severe in GaAs HBTs.

Throughout this paper, we will use a GaAs HBT sample-and-hold (S/H) circuit as an example. We will describe its thermal problems and the tools used to address them.

The Need for Thermal Simulation

Example: A GaAs HBT S/H Circuit

We designed and laid out an HBT sample and hold circuit (S/H), attempting to keep the device junction temperatures below 150°C . Assuming a maximum heatsink temperature of 80°C , this allows an on-chip temperature rise of up to 70°C . We estimated the thermal resistance of individual HBT devices using the expressions found in [4] and designed the circuit to keep the self-heating rise of each device below 40°C . At the time, we had no way to

calculate proximity heating (how much each device heats up its neighbors) and the circuit was laid out as densely as allowed by the design rules. The power in the core area ($600 \times 400 \mu\text{m}$) is about 2 W.

Initial testing of the fabricated circuit indicated very high operating temperatures and short device lifetimes. By comparison to deliberately overheated single transistors and resistors, we estimated that the highest junction temperatures in the S/H were in excess of 300°C . This stimulated the development of a software tool for thermal calculations which we call ThCalc [5].

Measurement Techniques

In general, experimentally verifying that safe operating limits are met is a difficult task because direct measurement of device junction temperatures is possible only for discrete test devices. Measurement of surface temperatures is possible in several ways, such as infrared or liquid crystal thermal mapping, but these are difficult techniques to use and they do not directly show the device junction temperatures. Because of the small size of modern transistors and the poor thermal conductivity of the dielectric layers used between interconnect levels, surface temperatures are often much lower than the junction temperatures. In addition, these techniques are applicable only after a chip has been designed, laid out and fabricated.

Electrical measurement of transistor junction temperatures is possible only when the device's terminal voltages and currents can be measured accurately; this is not generally possible for devices within a working circuit. So electrical measurements are generally limited to test devices, either standalone or embedded in a chip as temperature probes. This allows the test devices to be measured, but does not allow one to ensure that no devices on a chip are overheated.

ThCalc

We address this problem by providing a tool that can calculate the thermal rises that will exist throughout an IC while it is in operation. Once the predictions of such a calculation tool are verified against measurement, the tool may be used both to test whether existing designs are safe, and to aid in creating new designs that are optimized for minimal thermal effects.

Once configured and calibrated for a specific IC process, our tools extract the device geometries from the layout database and the power dissipated in each device from a spice simulation. This information is given to ThCalc, which calculates the temperature anywhere on the surface of the chip. The IC designer then uses this information to modify the chip design as necessary to ensure safe operating temperatures.

Although the example used in this paper is a GaAs HBT IC (the technology most in need of thermal simulation) we also use ThCalc on our silicon bipolar chip designs. ThCalc is also perfectly applicable to FET technologies, including CMOS, although the simulation of a large CMOS chip would require further speedups of the program or the computer used to run it.

The major problem with simulating CMOS circuits is in creating the input to ThCalc, which needs the power dissipated in each device. Since most of the power in a digital CMOS chip is dynamic switching power, the power in a particular device depends heavily on how often it is switched as well as its capacitive load. These depend on both layout and the data flow through the chip, which makes device powers hard to compute with much confidence. By contrast, many kinds of bipolar circuits are essentially constant-current circuits, so device powers may be simply estimated from the DC bias conditions (i.e., from a SPICE simulation).

Inside ThCalc

Physics

In general, static temperatures obey the Poisson equation [4]:

$$\nabla \cdot (k \nabla T) = -\dot{q} \quad (1)$$

where k is the thermal conductivity of the medium, $T(x,y,z)$ is the temperature and $\dot{q}(x,y,z)$ is the power generation per unit volume in the medium.

There are various known methods for solving this equation, both analytical and numerical, but most assume that k is independent of T . However, this is not true for semiconductors. The thermal conductivity of GaAs is roughly

$$k(T) = k(T_0) \left(\frac{T}{T_0} \right)^n \quad (2)$$

where $k(300K) = 0.44$ W/cm-K and n is about -1.25 [4], [6]. This means that the thermal conductivity of GaAs decreases by 30% between 25 and 125 °C. Silicon's thermal conductivity is about three times higher, but has a similar temperature dependence.

This would seem to invalidate the known methods of solving the Poisson equation. It can be shown, however, [7] that we can reduce the above two equations to the standard (constant- k) Poisson equation with a change of variables:

$$\tau = T_0 + k^{-1}(T_0) \int_{T_0}^T k(T') dT' \quad (3)$$

The pseudo-temperature τ now satisfies the constant- k form of the Poisson equation and the usual solution

methods apply. This allows us to solve for temperatures assuming a constant k and to use superposition to account for multiple heat sources. We may then transform back to the the real temperature rise ΔT (above the chip backside temperature T_0) via

$$\Delta T = T_0 \left[\left\{ \frac{(n+1)(\Delta \tau + T_0)}{T_0} - n \right\}^{\frac{1}{n+1}} - 1 \right] \quad (4)$$

where n is the exponent (about -1.25) used in (2).

Standard Solution Methods

Since Poisson's equation also describes electrostatic fields, there is a lot of literature on its solutions. The well-known methods of solving Poisson's equation include

- closed-form analytic solutions
- numerical Fourier series-summation methods
- numerical finite-element/finite-difference solutions

Closed-form analytic solutions are obviously the most attractive, but the only relevant result seems to be the solution for a point (or hemispherical) source on the surface of a semi-infinite medium:

$$T(r) = \frac{P}{2\pi kr} \quad (5)$$

where P is the source power and r is the distance from the source to the point in question.

When we add the boundary condition of constant temperature at the backside of a chip, however, it seems that there are no closed-form solutions. This brings us to series-summation solutions. Two such programs [8] [9] were tried, but the series convergence, even for sophisticated summation algorithms, is very slow. These programs may require hours to calculate temperature profiles consisting of only one source and a few dozen calculation locations (using a 14 MIPS workstation).

As with the series-summation programs, finite-element and finite-difference simulators [10] [11] [12] can provide important results for simple cases, but are also far too slow for full-chip profiles. In addition, they require large amounts of memory (16 to 48 MBytes for a single-device simulation), making simulations of even SSI chips impractical.

ThCalc's Method

ThCalc provides a computationally-efficient solution by taking advantage of the relatively simple set of geometries needed to represent heat flow in integrated circuits. It may be thought of as a series of simple steps:

- 1) Start with the analytic solution for a point heat source in a uniform medium (this will be a pseudo-

temperature).

- 2) Integrate in 2 dimensions to model a flat rectangular source.
- 3) Add empirically-determined corrections to account for finite substrate thickness, die attach layers, surface layers, chip edges, etc.
- 4) Add up the contributions of multiple heat sources (superposition) to obtain total pseudo-temperatures.
- 5) Transform from pseudo-temperatures to real temperatures to account for the semiconductor's temperature-dependent thermal conductivity.
- 6) Simplify where possible to speed up solutions without sacrificing much accuracy.

We start with the analytic solution for a point source, and integrate in x and y (the two dimensions in the plane of the chip's surface). This gives a complicated expression for the temperature distribution on the surface of a semi-infinite medium due to a rectangular ($w \times l$) source [4]. (In the far-field ($r > \sqrt{w^2 + l^2}$) we revert to the simpler point-source solution for greater speed.)

Next, we account for the effects of a finite substrate thickness, where the source is at the top of the substrate, and the bottom surface is held at a constant temperature (i.e., an ideal heatsink). It was found that for substrate thicknesses larger than the source dimensions, the infinite-substrate surface temperature distribution ($\propto \frac{1}{r}$)

should be multiplied by $e^{-\frac{r}{h}}$ where h is the substrate thickness and r is now the horizontal distance from the source to the calculation point ($r = \sqrt{x^2 + y^2}$). This provides a very close match to results from the finite-difference and series-summation programs. For this and most of the other empirical expressions, the finite-difference electrostatics simulator Fcap3 [11] [12] was used as the main standard of comparison. Pamin [9] was the series-summation (actually, Fourier integration) program used. (Note that ThCalc only calculates temperatures near the semiconductor surface; the above correction factor does not hold near the backside of the chip.)

For a source with dimensions comparable to the substrate dimensions, ThCalc breaks the source down into smaller pieces and treats them as separate sources. As a check, we note that in the limit for sources much wider than the substrate thickness, ThCalc does converge to the parallel-plate limit, albeit with a great deal more computation.

Next, we wish to account for extra layers beneath the chip, e.g., an epoxy die-attach layer. This contribution was derived exactly from the point-source, finite-substrate expression described above for the case of the second layer

having the same thermal conductivity as the first. Empirical correction factors for different values of thermal conductivity were then added in. The resulting expression is

$$\Delta\tau_2(r) = \frac{P}{2\pi k_2 r} \left[e^{-\frac{r}{\left(\frac{k_1}{k_2}\right)^{1/4} h_1 + h_2}} \right] \left[1 - e^{-\frac{r h_2}{\left(\frac{k_1}{k_2}\right)^{1/2} h_1 (h_1 + h_2)}} \right]$$

where k_1 and h_1 refer to the semiconductor substrate and k_2 and h_2 refer to the die-attach layer. This is found to match well with finite-difference simulations for all "reasonable" cases of die-attach layers (to be explicit, when $h_2/h_1 < 25k_2/k_1$).

The effect of chip boundaries may also be included in the simulation. These effects are included by the method of images [13] which is commonly used in electrostatics: the effect of a thermally reflecting boundary (such as a chip edge) may be modeled by adding a fictitious "image" source reflected perpendicularly across the boundary. By summing the effect of the real source and the image source, the effect of the boundary may be calculated exactly. When we have two parallel boundaries (e.g., the right and left edges of a chip) the method of images calls for an infinite array of image sources (the boundaries reflect images of each other). Fortunately, because of the

exponential factor $e^{-\frac{r}{h}}$ due to finite substrate thickness, only image sources quite close to the chip boundaries need be included. Therefore, each source in the chip is mirrored about the four chip edges to create a 3×3 array of sources (the original and 8 images). For all practical cases (chip thickness less than the horizontal dimensions) the use of 8 images is completely sufficient. The drawback to using this feature is that it increases computation time by the same factor of 9. For many chips, this step may be omitted with a relatively small impact on simulation accuracy.

For verification purposes, it is also useful to predict temperatures at the top of the dielectric and encapsulation layers of the finished IC. These predictions can be compared directly to infrared or liquid crystal surface temperature measurements. For this purpose, we modify r , the horizontal distance from the source to the calculation point to allow small values of z :

$$r = \sqrt{x^2 + y^2 + z^2}$$

In practice, the value of z used is chosen to best fit the temperatures seen in finite-difference simulations of device, interconnect and intermetal dielectric layers. In fact, even for junction temperature calculations, the value of z is typically in the range of 0.5 to 1.5 μm to account for the effects of non-flat device geometries and the cooling effects of interconnect metal.

It is important to note that although several empirical expressions are used in the program, the value of z is the only “fudge factor” in the model. All other parameters given by the user are simply physical descriptions of the chip and layout geometries.

Correcting for Temperature-dependent Thermal Conductivity

The above calculations produce the pseudo-temperature τ for one source. After adding together the contributions from all the heat sources, we then convert these calculated pseudo-temperatures to real temperature rises using equation (4) above.

The contributions of non-semiconductor layers are handled separately: the thermal conductivity of these materials is generally fairly independent of temperature, so their contributions are left unchanged in this step. This is not strictly correct; the transform of equation (3) is valid only for a uniform medium. In the cases of practical interest, however, the thermal rise in the packaging materials is usually small compared to the rise across the semiconductor, so the error is negligible.

Performance Tricks

As mentioned earlier, the complicated expression for a rectangular source is used only in the vicinity of the source. Once the calculation point is far enough from the source, we use the simpler point-source expression.

The other major performance feature of ThCalc is the grouping of sources by physical location. The number of groups varies between 30 and 200 depending on the number of sources. ThCalc finds the weighted center of all the power sources in each group, and uses that as a single source to represent all the sources in the group when the distance from the group edge to the calculation point is more than 1.5 group widths. This simplification leads to about a $7\times$ speedup in ThCalc for a 2400-device (silicon) chip. It also reduces the $9\times$ runtime penalty for using the method of images to 2 to $5\times$. The loss in accuracy is only about 1%.

Verification of ThCalc

Characterizing a New Process for ThCalc

To fully characterize a new process for ThCalc, we need to choose a value of z for each type of power-dissipating device (transistors, diodes, resistors). Detailed Fcap3 models of individual devices are built and run for several different dimensions of each device. The ThCalc z parameter is then adjusted for each device to give the best fit to the Fcap3 results. The values obtained usually are 1 to 3 times the physical z -dimension of the devices' power-dissipating region, but also depend on whether the power region is buried or on the surface of the semiconductor,

and what interconnect metal geometries are typically used. This characterization process can be skipped, of course, and guesses or even a value of 0 can be used for z . The value of 0 is guaranteed to be conservative, since this corresponds to the highest power density case, a flat 2-dimensional power region. This will exaggerate the temperature rise of each device due to self heating, but not change the proximity heating between devices.

Comparison to Other Tools

Figure 1 shows the thermal profile of a $2.2 \times 2.2 \mu\text{m}$ source on a $75 \mu\text{m}$ thick substrate, attached with $50 \mu\text{m}$ of epoxy to a perfect heatsink, as calculated by Fcap3, Pamin, and ThCalc (after choosing z for best match to the Fcap3 results). (The device dimensions were chosen to exercise the tools rather than represent real devices. Also, ThCalc's correction for temperature-dependent thermal conductivity was turned off to allow direct comparison to the other simulators). All three simulations agree quite well. ThCalc, however, runs over 100,000 times faster than either of the more general simulators and takes little memory.

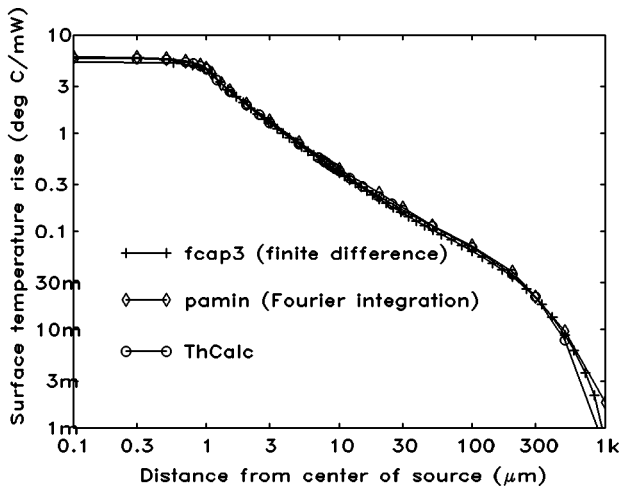


Figure 1: Fcap3, Pamin and ThCalc: $2.2 \times 2.2 \mu\text{m}$ source,
 $h_{\text{semi}} = 75 \mu\text{m}$, $h_{\text{epoxy}} = 50 \mu\text{m}$

HBT Junction Temperatures

Detailed 3-dimensional descriptions of two HBT devices were entered into Fcap3 and simulated. The predictions of Fcap3 are compared to measured [14] temperature rises for those transistors in Figure 2. The temperature-dependent thermal conductivity of the semiconductor is demonstrated by the upwards bend of the lines (the Fcap3 results have been post-processed to include this effect, too). The agreement is within 3% for the small device and low by 17% for the large device. This is not as close as we would like, but is adequate for most purposes.

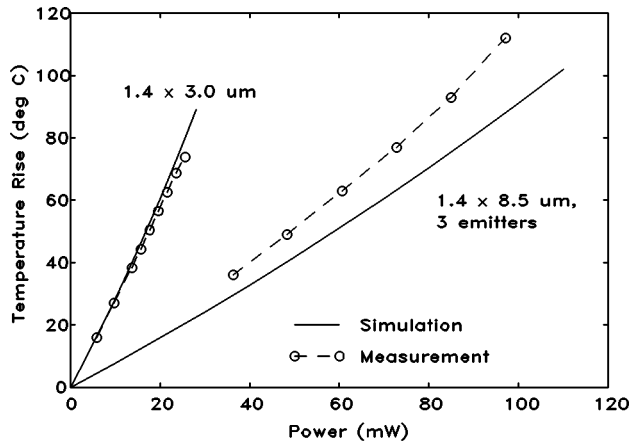


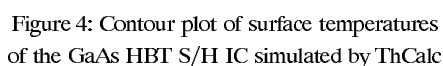
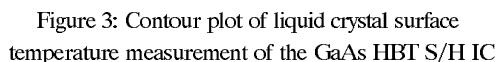
Figure 2: Measurement and simulation of temperature rise in two HBT devices.

With this confirmation of Fcap3 modeling of individual transistors, we choose ThCalc's z parameter to make ThCalc's simulation results match the Fcap3 results. The NiCr resistors in this process are on the order of 100 Å thick, so a z of 0 is appropriate for these devices when simulating device temperatures. We then proceed to simulate temperature profiles of circuits.

S/H Chip Surface Temperatures

An HBT chip was measured by the liquid crystal technique; the result is shown in Figure 3 (not all of the contours have been drawn in, and none were measured below a rise of 90 °C.). The heat sources (transistor emitters and resistors) are shown also. The same chip was simulated with ThCalc; the result is shown in Figure 4. The dielectric layers above the devices reduce the surface temperatures well below the junction temperatures, so new z values for the transistors and resistors were obtained by matching ThCalc simulations to the surface temperatures seen in Fcap3 simulations. The liquid crystal measurement was marred by difficulty in getting stable transitions in the liquid crystal material at high temperatures and by

Fri Aug 30 12:51:18 PDT 1996



These plots, of course, are of surface temperatures (above the scratch-protect layer). What we really need to predict are temperatures at the device junctions, since this is where heat-induced failures actually occur. On the same HBT IC, we observed resistor burnout on four resistors (shown near the center of Figure 4). This occurred only on the wafers with the highest currents (due to low resistor sheet resistance). When we modeled operating conditions for these wafers, we computed surface temperatures above these resistors of about 155 °C, but internal device temperatures for these resistors were computed to be 420 °C. (The large difference between device and surface temperatures is partly due to the use of polyimide for the

intermetal dielectric, which has a thermal conductivity of .0015 W/cm-°C, about 10x smaller than SiO₂.) Later measurements of test resistors confirmed that resistor burn-out occurs at internal temperatures of 390 to 520 °C.

Also on the same IC, a diode added to the circuit as a temperature probe shows a rise of 100 to 120 °C (by V_{BE} measurements). ThCalc predicts 104 °C.

Using ThCalc for Design

ThCalc's input is a text file listing the location, size, power and type of each device in the chip. For early stages of a design, this list may be constructed by hand, at least for small parts of a chip. During or after the layout phase, it can be extracted from the chip database. We wrote one tool which extracts the device locations and sizes from our artwork database and another which finds the power in each device using a SPICE simulation. These are merged together to form the input file for ThCalc.

The two forms of output from ThCalc are a text listing of the peak temperature in each device, and contour plots of the temperatures in the chip. The contour plots give the designer an intuitive feel for the locations of the major concentrations of power. The text listings are sorted by temperature to highlight the devices with the highest temperatures. ThCalc thus provides both qualitative and quantitative feedback on circuit temperatures. This allows the designer to concentrate on reducing temperatures only in the hot spots.

Running ThCalc to generate the list of device temperatures for a 2400-device chip took about 4 minutes on a 14 MIPS workstation; the contour plot took about an hour.

To reduce the peak temperatures in bipolar ICs, several strategies are available (roughly in order of increasing cost and disruption to the circuit design):

- use device layouts with narrower emitters (with the same area) and/or wider spacing between emitters
- spread devices farther apart from each other
- decrease device current density (increase emitter or resistor area)
- reduce the power dissipated in the circuit
- change the packaging (thin the substrate, change die attach and package materials, heatsinks, etc)

Typical usage of ThCalc in a chip layout is to first perform a layout which is optimized for best speed and density. ThCalc is run on the resulting layout to find regions that may exceed the process temperature limits, and the regions with problems are then adjusted using the above four strategies until the circuit meets the process temperature limits. During this process, ThCalc must generally be run for a variety of operating conditions (e.g., with key

input signals at their high, nominal and low points) to attempt to simulate all the worst cases. ThCalc may also be run with different parameters for the die-attach and package layers to aid in evaluating packaging options. A key advantage of ThCalc over the methodology of [15] is that ThCalc's use of empirical equations based on physical layer dimensions and properties eliminates the need for a library of substrate and package structures previously simulated with a finite-element or Fourier-integration program and fitted to the equations in the calculation program.

Application to the S/H Circuit

We used ThCalc to calculate the temperatures in the original layout of the HBT S/H chip. The thermal contour plot of device junction temperatures is shown in Figure 5. Note that Figure 4 is a plot of surface temperatures (on top of the dielectric layers) used only to compare to the liquid crystal measurement. Figure 5 is more typical of the designer's use of ThCalc - it shows device junction temperatures within the devices and temperatures at the semiconductor surface in between devices.

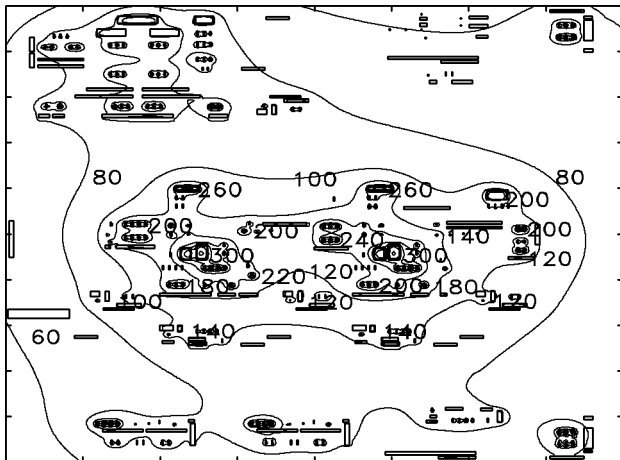


Figure 5: Simulated temperature profile of device junction temperatures of the GaAs HBT S/H

ThCalc predicted that the highest device temperature rise on the S/H chip will be about 300 °C on a pair of resistors near the center. This agreed with the location of visible thermal damage to the polyimide layer over the chip, which is expected to begin at around 250 °C. Destructive testing of some S/H chips and single devices indicated that the predictions of ThCalc agree with measurement, though the uncertainties of these measurements were about 25%.

We then used ThCalc to calculate the temperature reductions possible by using a 1 mil solder die attach (0.35 W/cm-°C) instead of the original 1 mil epoxy (0.018 W/cm-°C), and by backlapping the semiconductor substrate from 25 down to 3 mils. ThCalc predicted that

temperatures would reduced by over 100 °C if both of these steps were taken (see Table I), but this is still far from the goal of temperature rises less than 70 °C.

Layout	Substrate thickness (mils)	Die attach (1 mil)	Temperature Rise Hottest Resistor	Hottest HBT
original	25	epoxy	305 °C	255 °C
original	25	solder	225 °C	175 °C
original	3	solder	200 °C	112 °C
modified	25	epoxy	150 °C	154 °C
modified	25	solder	117 °C	118 °C
modified	3	solder	74 °C	71 °C

Table I: Simulated junction temperature rises (above heatsink temperature) before and after use of ThCalc.

Using ThCalc as a guide, the hottest areas of the S/H circuit layout were then modified using the first three strategies listed above. For the new layout, ThCalc calculates temperature rises of less than 75 °C. This represents a reduction in peak temperature rises by a factor of 1.6 to 2.7. These reductions were achieved with only a 25% increase in the area of the S/H core and negligible change to the simulated electrical performance. This demonstrates that large reductions in operating temperatures can be made with quite modest area increases when a tool such as ThCalc is available to show exactly where changes must be made.

Chips have been fabricated and tested using the modified layout. No visible evidence of overheating was observed, showing that all device temperatures are below the ~250 °C point where polyimide shows discoloration.

In the original layout a diode was placed near the center of the S/H to act as a temperature monitor; a second one farther away was added in the modified layout. Since these diodes are run at low currents, their self-heating is very small, so they act as good indicators of the proximity heating caused by other devices in the vicinity. A summary of the match between measured and simulated temperatures is shown in Table II. The resistor measurement is inferred from the burnout of resistors, which occurred only on high-current wafers. The simulation of diode temperatures all agree with measurements within 8 °C, which is quite adequate for most thermal design purposes.

It is interesting to note from Table II that temperatures are actually higher for the 3 mil thinned substrate than for the 25 mil substrate (this case was tried only for the purpose of testing ThCalc's predictions). This is due to the poor thermal conductivity of the epoxy die-attach layer; the thicker substrate acts as a heat spreader over the epoxy. To benefit from a thinned substrate, a solder or eutectic die-attach must be used (though we don't have measured data for this case yet). ThCalc correctly predicts this effect. This data completes the verification of ThCalc against measurement.

Sensor	Chip	Substrate thickness (mils)	Die attach (1 mil)	Temperature rise above heatsink	
				Sim	Msmt
resistor	original	25	epoxy	400 °C	450±60 °C
diode1	original	25	epoxy	104 °C	110 °C
diode1	modified	25	epoxy	24 °C	28 °C
diode1	modified	3	epoxy	109 °C	105 °C
diode2	modified	25	epoxy	12 °C	12 °C
diode2	modified	3	epoxy	63 °C	55 °C

Table II: Comparison of various measured and simulated junction temperature rises (above heatsink temperature).

Summary

Maintaining safe operating temperatures is vital to all ICs, but is especially difficult for GaAs HBT circuits. These circuits virtually require thermal simulation to ensure that they operate at safe temperatures. We wrote a new simulation tool called ThCalc to efficiently calculate integrated circuit temperature profiles from design data; its results show good agreement with the experimental data. It is about 5 orders of magnitude faster than more general kinds of simulators and uses only one non-physical input parameter.

We used ThCalc to guide the re-layout of an HBT S/H chip to ensure that safe operating temperatures were maintained. Large reductions of peak junction temperatures were achieved with only a modest increase in die area.

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Figure Captions

Figure 1: Fcap3, Pamin and ThCalc: $2.2 \times 2.2 \mu\text{m}$ source, $h_{\text{semi}} = 75 \mu\text{m}$, $h_{\text{epoxy}} = 50 \mu\text{m}$

Figure 2: Measurement and simulation of temperature rise in two HBT devices.

Figure 3: Contour plot of liquid crystal surface temperature measurement of the GaAs HBT S/H IC

Figure 4: Contour plot of surface temperatures of the GaAs HBT S/H IC simulated by ThCalc

Figure 5: Simulated temperature profile of device junction temperatures of the GaAs HBT S/H

Table I: Simulated junction temperature rises (above heatsink temperature) before and after use of ThCalc.

Table II: Comparison of various measured and simulated junction temperature rises (above heatsink temperature).

Ken Poulton (M'80) was born in Oakland, CA in 1956. He received a B.S. in physics and an M.S. in electrical engineering from Stanford University in 1980. While at Stanford, he worked at Ampex in Redwood City, CA on SAW devices.

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Thermal Design and Simulation of Bipolar Integrated Circuits

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