GHz ADCs: From Exotic to Mainstream

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Outline
A Quasi-Chronological View of GHz ADC Architectures

Flash

Folded and Interpolated

Time Interleaving

CMOS

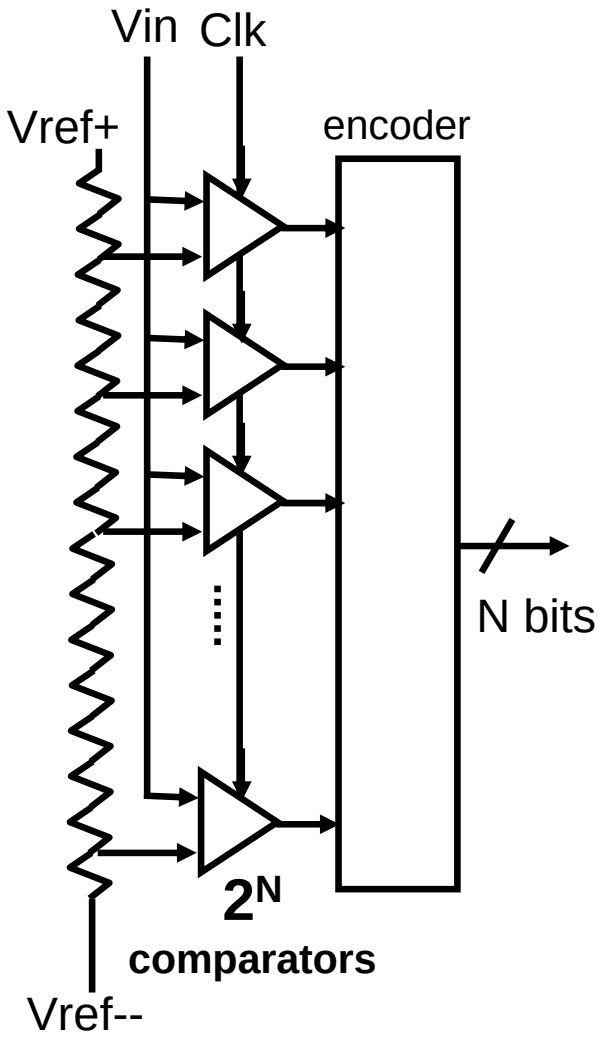
Massive Interleaving

Flash, Folding, SAR

Architecture: Flash ADC

In the beginning, there was the Flash.

And it was not so good.



+ Fastest ADC architecture: all parallel
+ Lowest latency
-- power and transistor count of 2^N comparators limited this to ~4 bits for fast ADCs
  - 3 W was a high-power chip
  - 1000 BJTs was near process yield limit

So the first GHz ADCs were Folding (or Folded Flash)

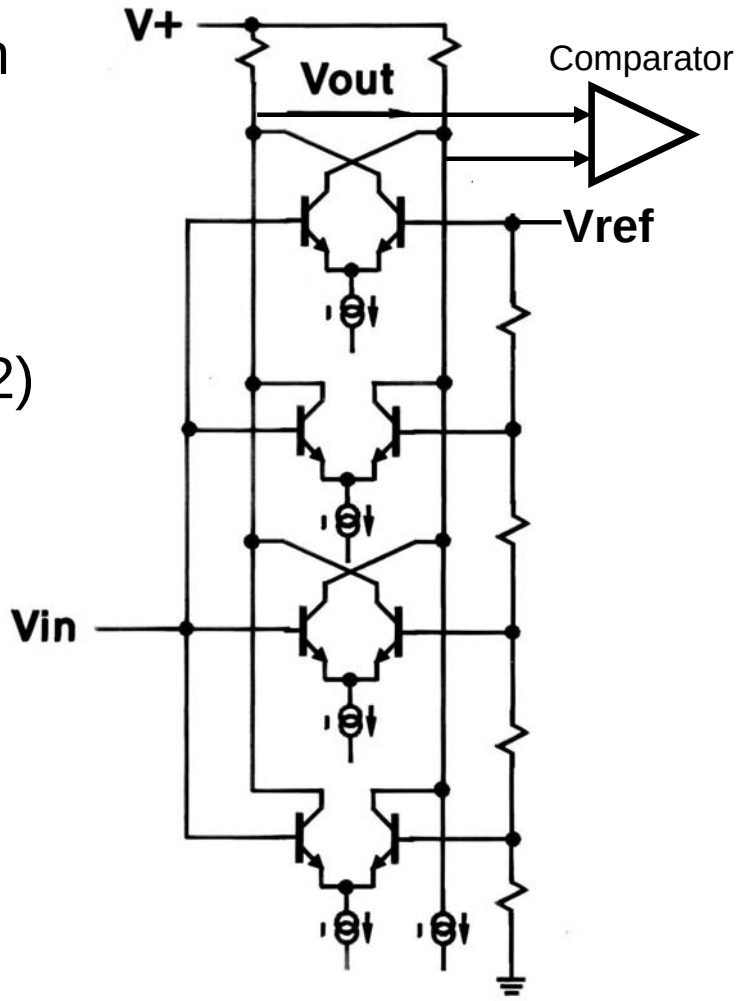
Architecture: Folding ADC

Reduce the number of clocked comparators:

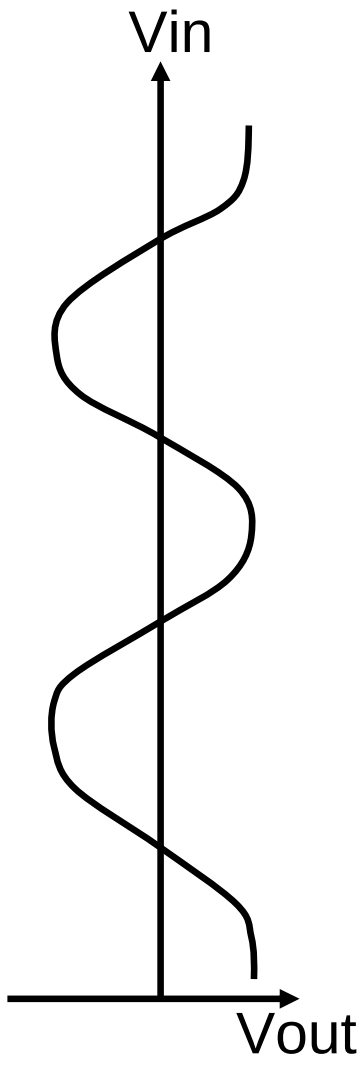
- Put an analog folding circuit in front of each comparator
- Each comparator is used at multiple zero crossings
- Add MSB comparators (e.g., 2) to determine which zero crossing

van de Plassche & Grift, "A 7b A/D converter", ISSCC 1979, **50 MSa/s**

Analog Folding Circuit



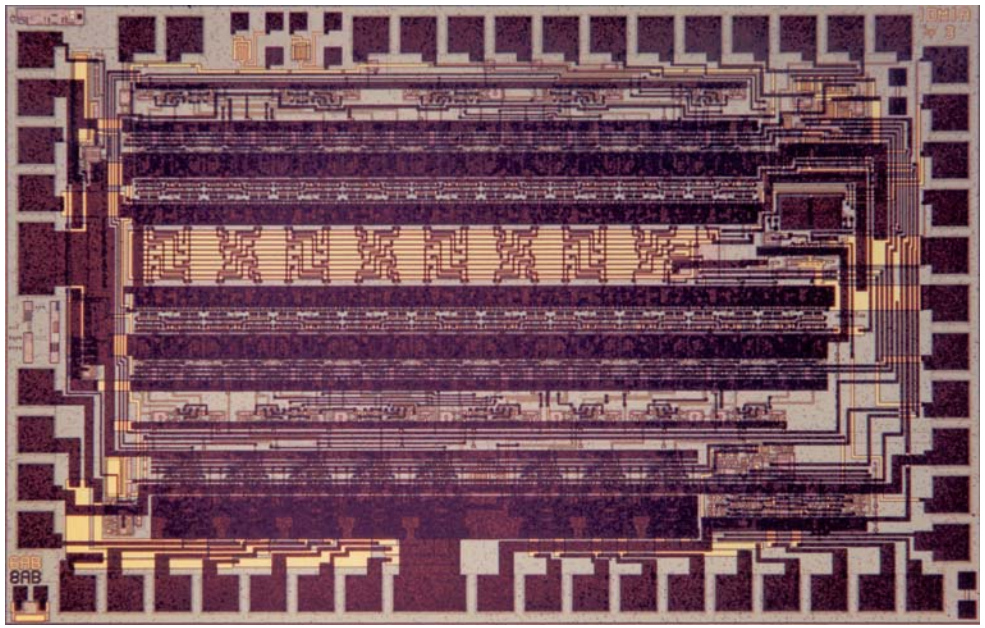
Transfer Function



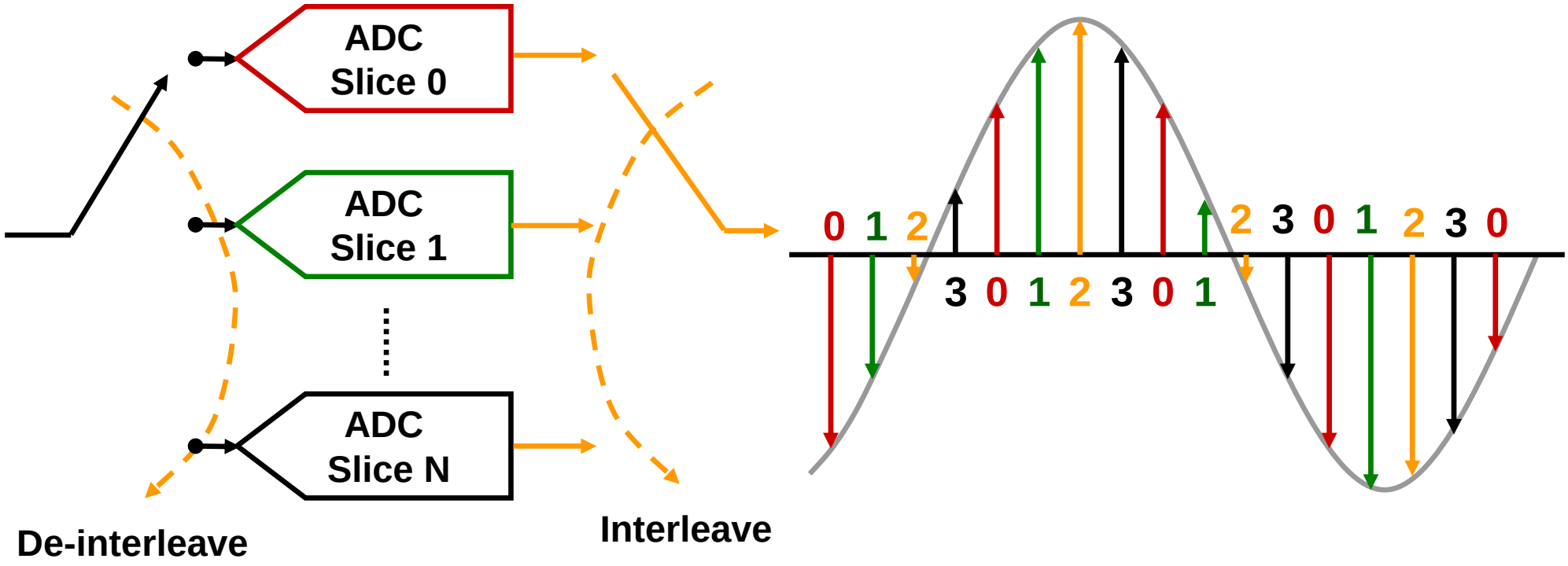
1984: 0.4-GSa/s 6-bit ADC

Corcoran, Knudsen, Hiller, Clark “a 400 MHz 6b ADC”, ISSCC 1984

- 400-MSa/s 6-bit ADC
- 850 transistors in a 5-GHz f_T bipolar process (2.5 um)
- 5.8 effective bits at 100 MHz Fin, 2.7 W
- 4-way folding to reduce the comparator count from 63 to 17
- Used in the HP 54102A oscilloscope – the first realtime digital scope



Architecture: Time-Interleaved ADCs

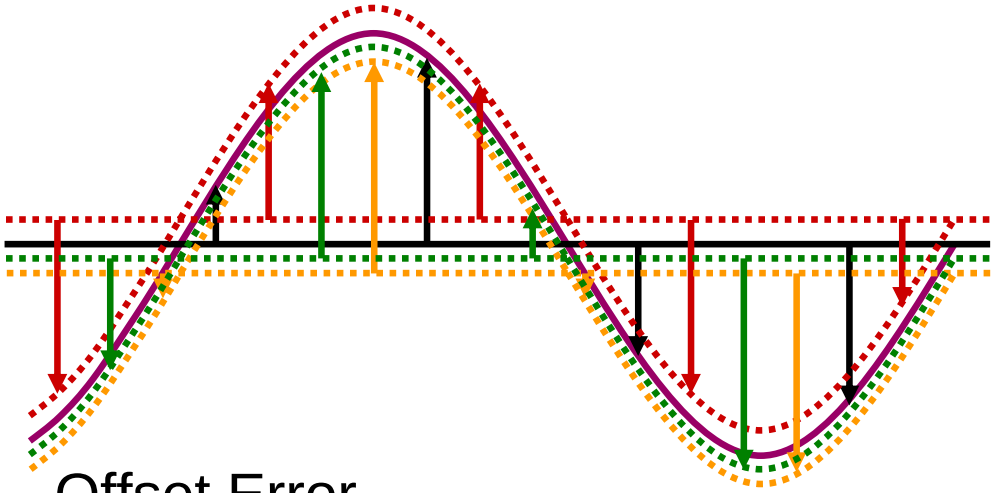


ADC/Quantizer speed is limited by comparators and amplifiers.

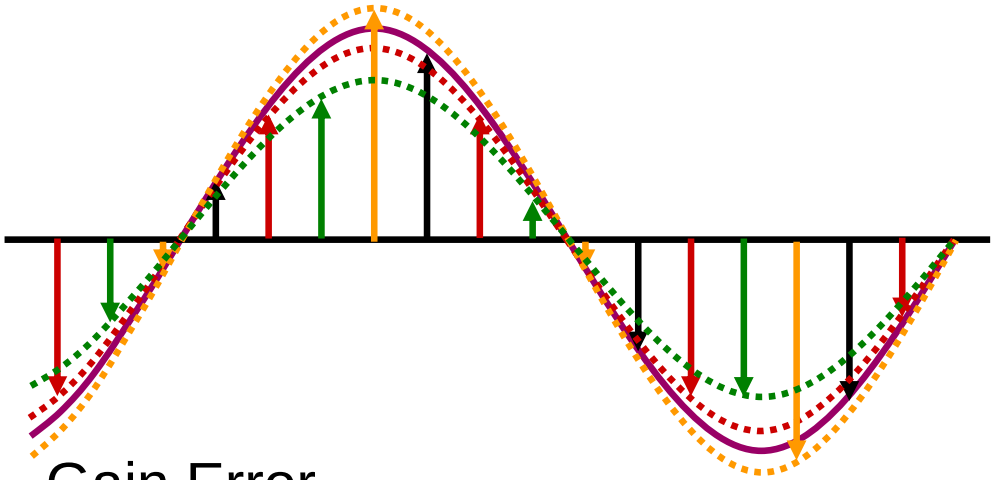
Interleave multiple low speed ADCs (called slices) to increase effective sampling rate.

ADC slices need to be very well matched in **offset, gain, sample time and bandwidth**

Interleaving Errors



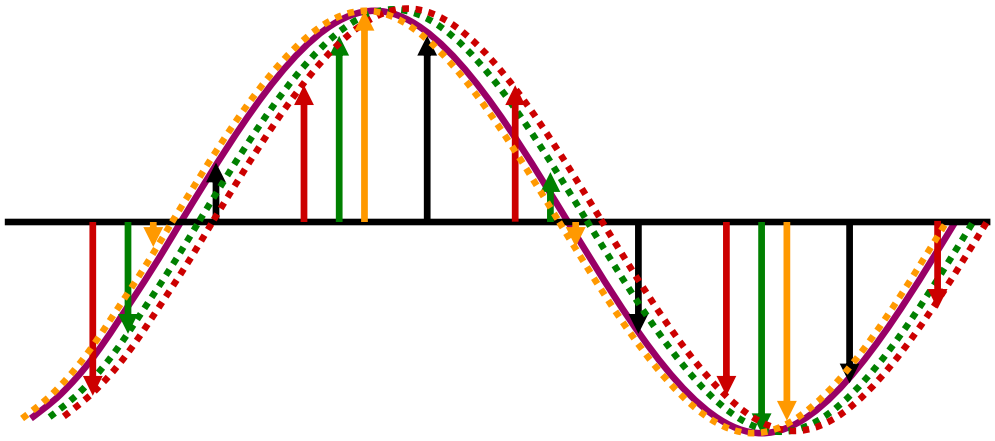
Offset Error



Gain Error

Errors due to mismatched paths cause:

- Distortion and jitter in the reconstructed waveform
- Spurs in the spectrum

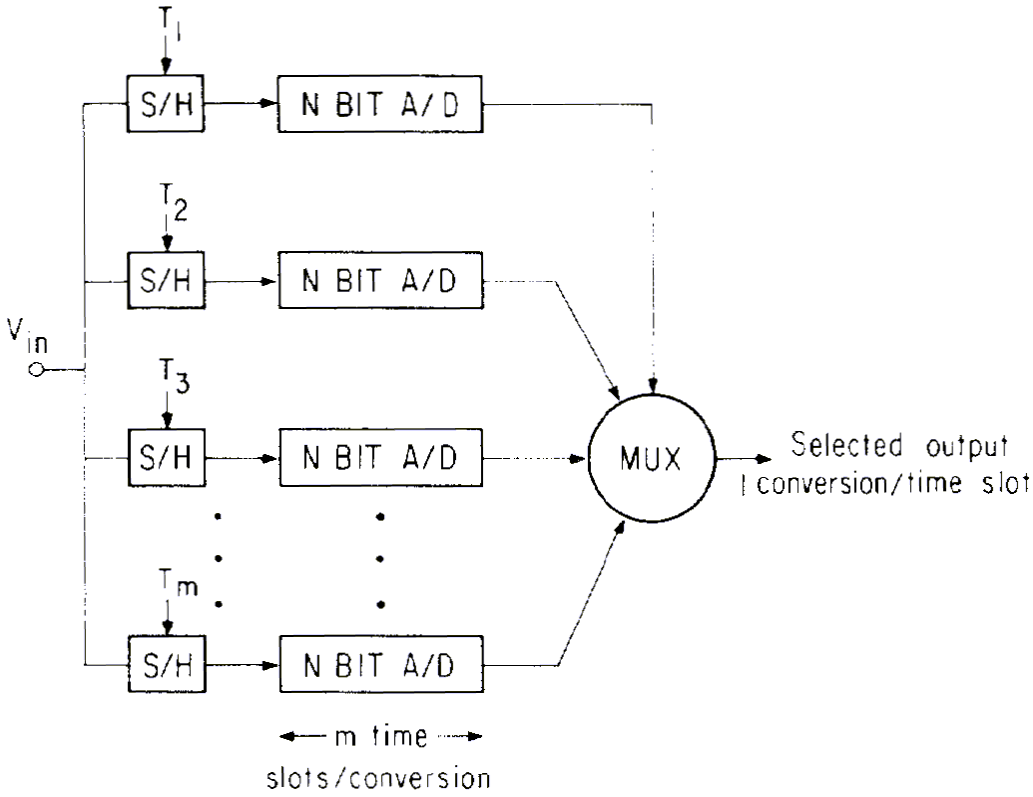


Sampling Instant Error

Time Interleaving – the first chip

Black & Hodges, “Time Interleaved Converter Arrays”, ISSCC 1980

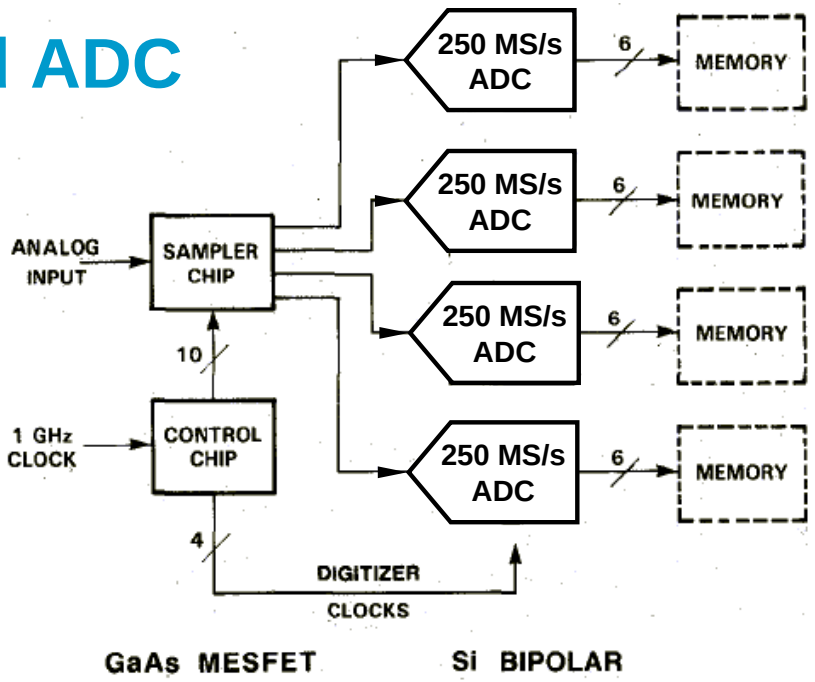
- 4-way time interleaving
- Parallel samplers
- Slice matching by design
- 7-bit SAR ADC slices
- **4 MSa/s** total (10-um CMOS)

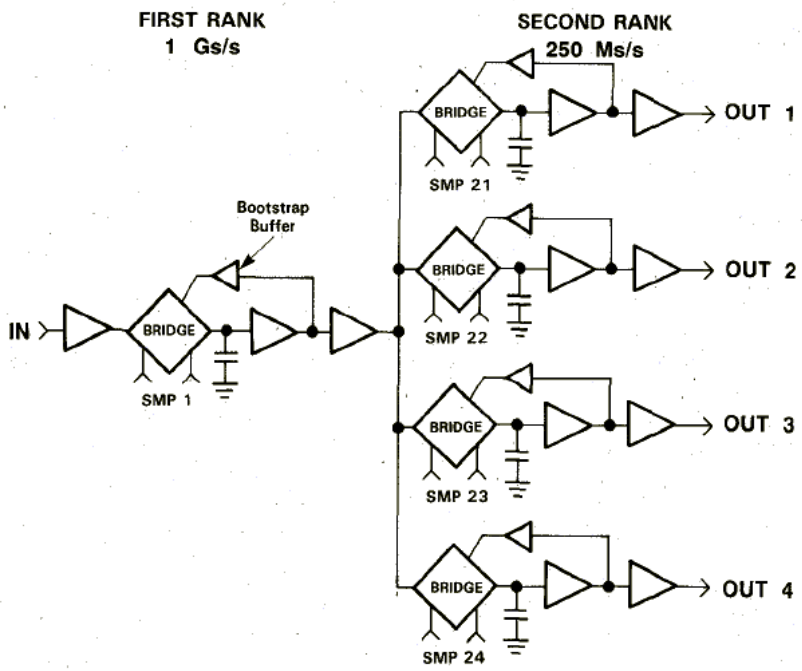


1987: The First Gigasample/second ADC

- Approach
  - Start with the fastest unit ADC possible
    - the previous bipolar ADC at 250 MSa/s
  - Interleave a few ADCs (4) to get 1 GSa/s
  - T/H circuits in a faster process
    - 13 GHz GaAs

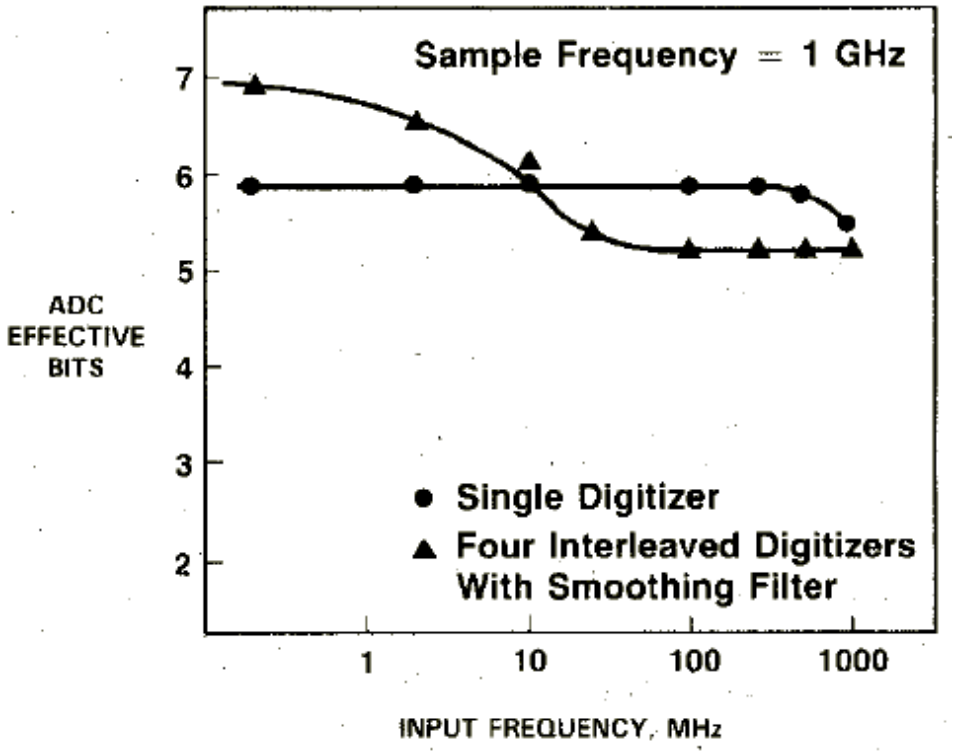
- Mismatch control
  - Offset and gain alignment by on-PCB pots
  - Single front-end sampler for timing alignment

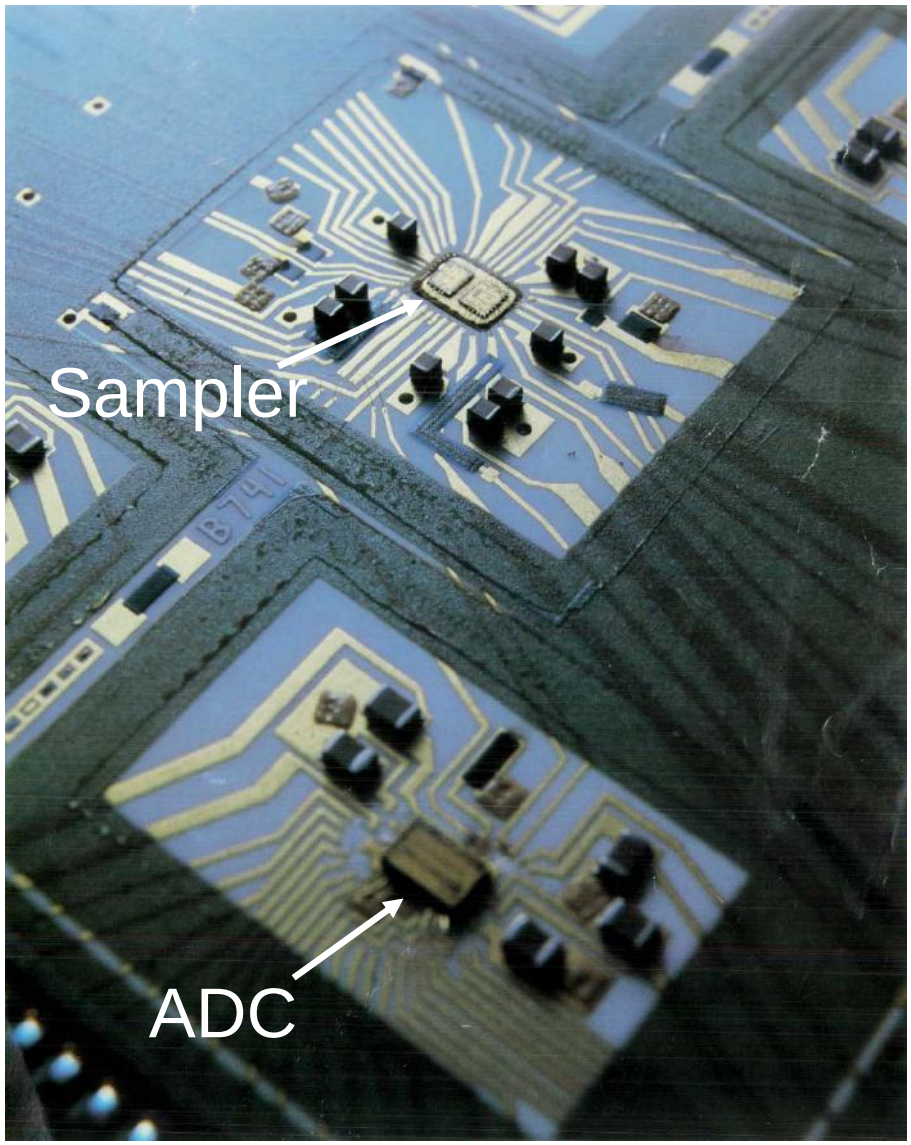




1987: The First Gigasample/second ADC

- 1 GSa/s, 1.7 GHz analog BW
- 10-chip system (with memories)
- 16 W
- 5.2 effective bits to 1 GHz F_{IN}

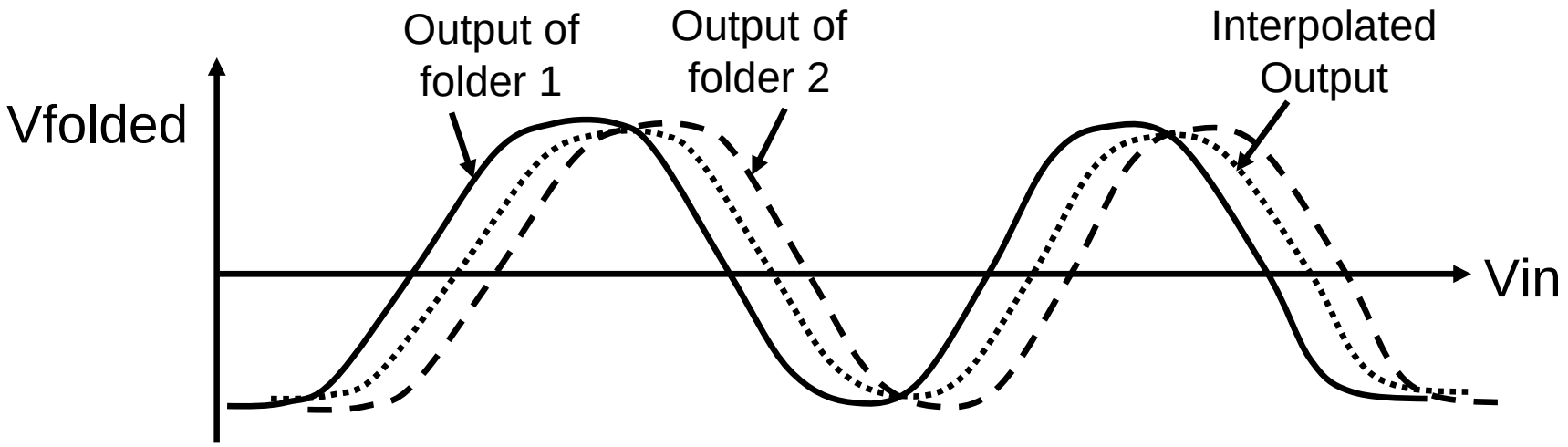




Architecture: Folding with Interpolation

van de Plassche & Baltus, “An 8-bit 100-MHz full-Nyquist analog-to-digital converter”, ISSCC 1988

- Observation: folding circuits dominate input loading (2^N total diff pairs for N-bit ADC)
- Adjacent folding circuits outputs differ by a shift in the Vin axis
- So reduce the number of folding circuits by interpolating between adjacent folders’ outputs with resistive dividers

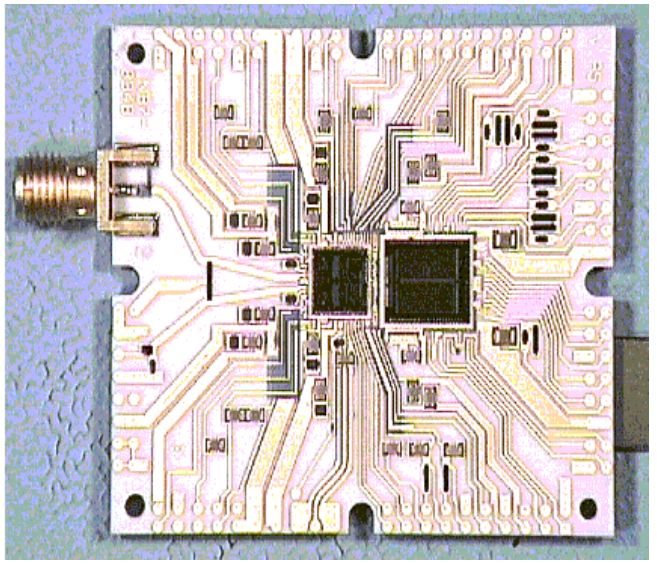


Characteristics of Gigasample ADCs in the 90s

- Mostly for Scopes
- Bipolar or HBT IC technology
  - Speed
  - Threshold Accuracy
- Designed for low transistor count
  - Yield
  - High power per transistor
- Highest possible slice sample rate
  - Time-interleaving of 2-4 unit ADCs
- Front-end T/H
  - Diode Bridge
  - Switched Emitter Follower
  - Sample + Filter
- High Power
- Custom Packaging

E.g.: 1997 4 GSa/s Module

- 4 GSa/s, 7-bit bipolar ADC
- Folding + Interpolating
- 2-way interleaving on chip, 4-way on board
- Custom CMOS Memory
- Thick-film package
- 13 W, expensive



Some Scope ADCs in the 90s

HP in 1991

Rush & Byrne, “A 4GHz 8b Data Acquisition System”, ISSCC 1991

- 500 MSa/s per slice, 1 GSa/s per chip, 13-GHz silicon BJT, folding ADC
- 4, 8-way interleaved to up 4 GSa/s

HP in 1994

Poulton, et al, "A 6-bit, 4 GSa/s ADC Fabricated in a GaAs HBT Process",1994 GaAs IC Symposium

- 4 GSa/s, 6 bits, 50-GHz GaAs HBT, folding ADC
- Did not go into a product

HP in 1997

Poulton, et al,“An 8-GSa/s 8-bit ADC System", VLSI Symposium, 1997

- 2 GSa/s per slice, 4 GSa/s per chip, 7 bits, 25-GHz silicon BJT, folding and interpolating
- 2, 4-way interleaved to 8 GSa/s

Other scope manufacturers

- developed bipolar ADCs, but did not publish
- followed the fast-slice, low-interleaving paradigm

Trends in the 90's

- Consolidation of IC fabs
  - In 1990, lots of captive IC fabs - HP had about 10 fabs
  - In the late 1990's, fab construction costs (~$1B) squeezed out many players
  - Commercial foundries with leading-edge CMOS gained much of this business
- Bipolar
  - Increasingly a niche technology, focused on performance
  - Investment driven by specific market trends
    - ~1990: CPUs, ~2000: RF, ~2010: 25+ Gb/s comms
    - Investment fades as CMOS gets fast enough for a given application
    - => Less predictable progress in bipolar
- CMOS – Moore's Law
  - Wafer costs much lower
  - With higher integration, system costs even lower
  - Predictable progress in performance

Could We Use CMOS for Scope ADCs?

“Don’t be stupid”

- CMOS ADCs (ca 1996) are 25-50 times slower than bipolar
- CMOS transistors are 10 times less accurate than bipolars

“But...”

- CMOS chips are cheap and transistors are virtually free
- Could integrate with DSP, memory, etc
- Might be lower power

"If we don’t do it in CMOS, someone else will.”

-- Dave Robertson, ADI

Architecture: Massive Interleaving of Low-Power ADCs

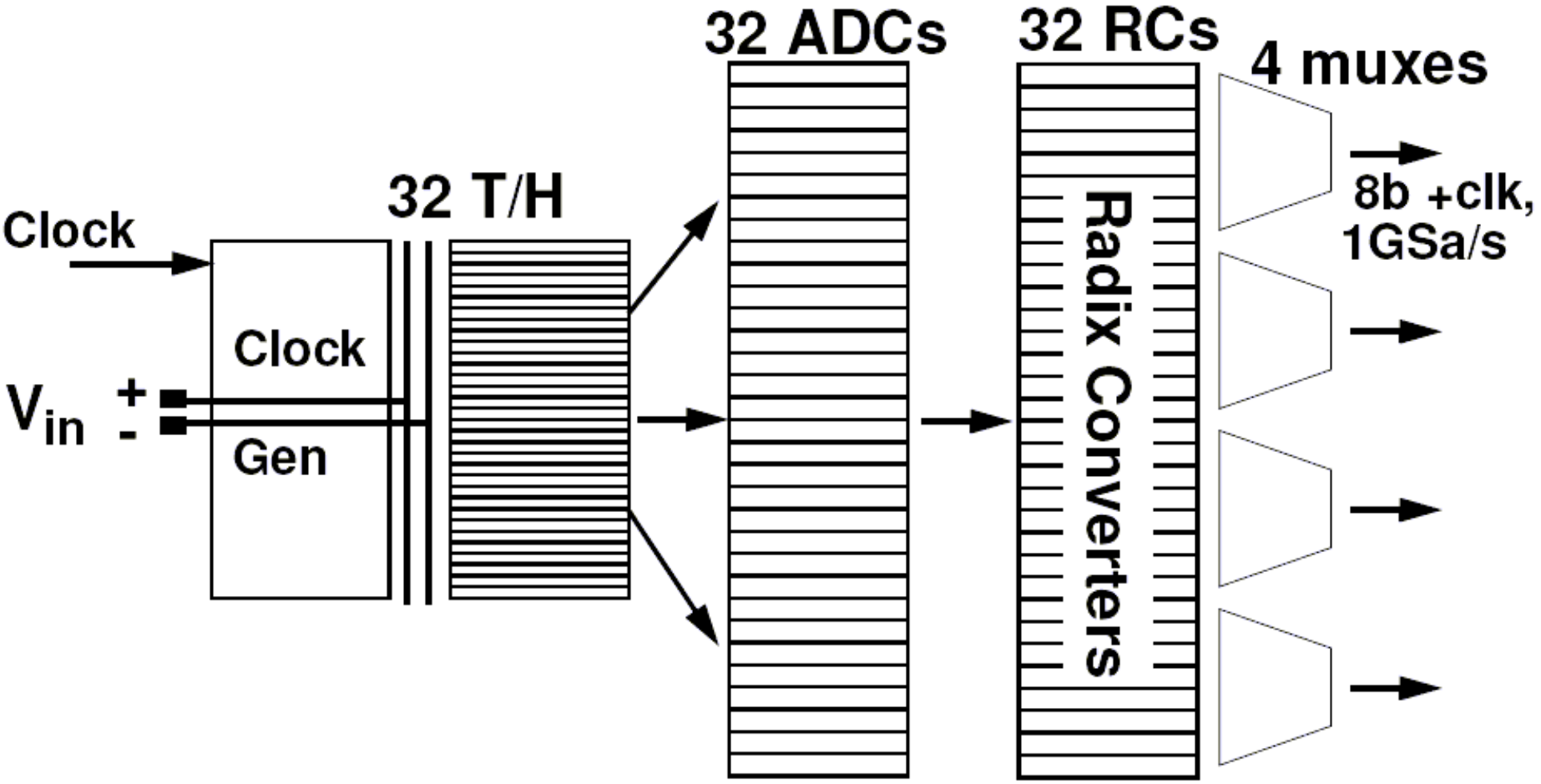
- Focus on the strengths of CMOS: low power and high integration
- Start with the most power-efficient CMOS ADC slice
- Time-interleave like crazy to get the required sample rate
- Fix up analog accuracy through calibration

Challenges:

Track/Hold : Bandwidth, Channel mismatch, Clocks

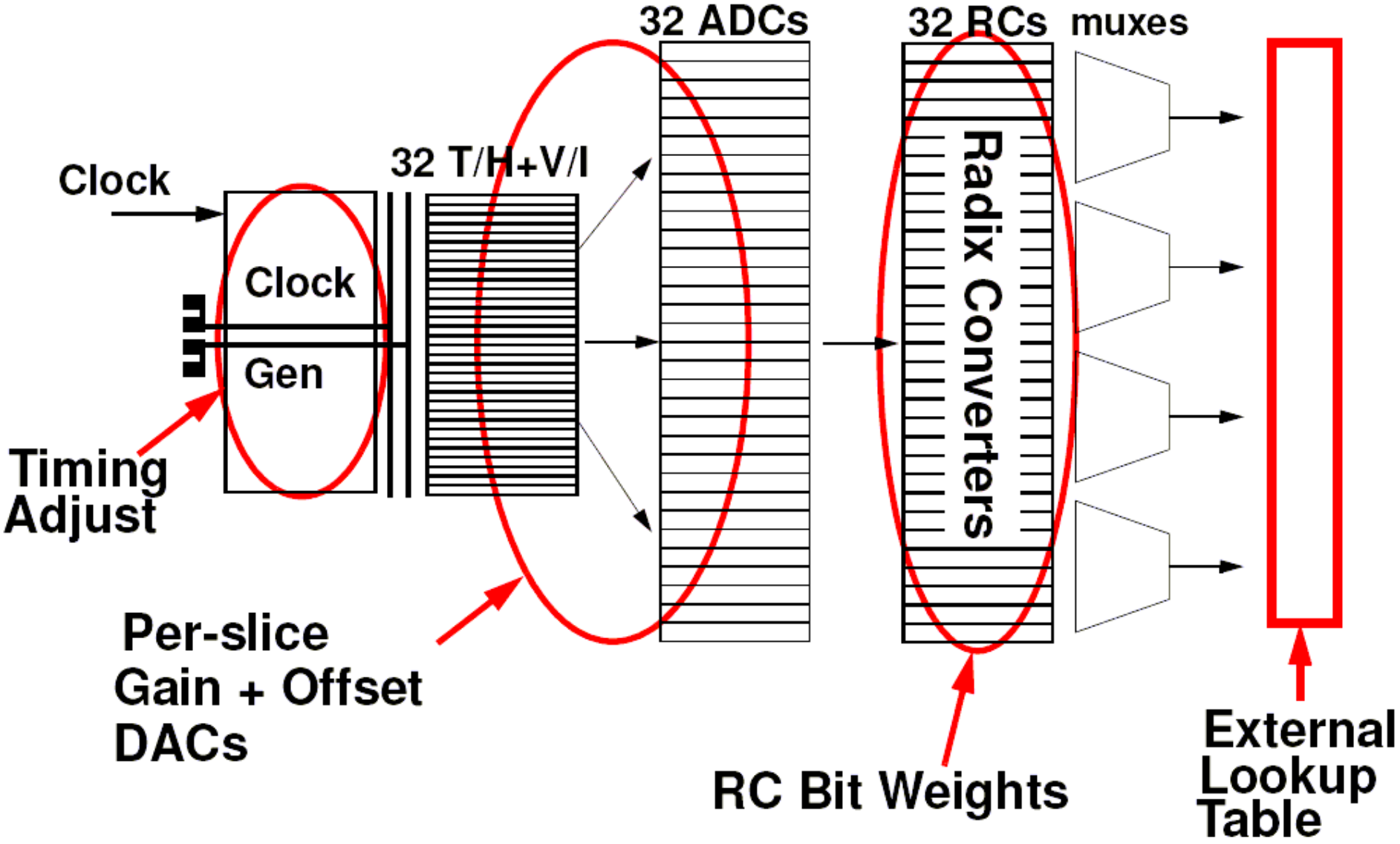
ADC: Sample Rate, Power/sample, Circuit area

2002: CMOS ADC Chip Architecture (4 GSa/s)



- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s

What Is Calibrated?



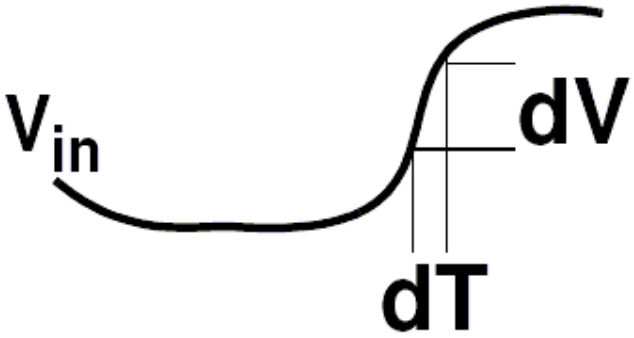
Offline Calibration with DC and Pulse sources

Advantages of a Calibration Approach

- Device mismatch tolerance increased
  - In this case, from ~0.25% to ~10% mismatch
  - Can design for SNR rather than mismatch
  - Circuit goes from large devices to quite small, power goes down
- Second-order effects can be covered by the same calibrations
  - Smaller device mismatch effects (e.g., layout-related delta W)
  - Delay and gain mismatches due to layout asymmetries
- Adjust DACs need not be tightly matched, merely have enough resolution

Timing Error and ADC Resolution

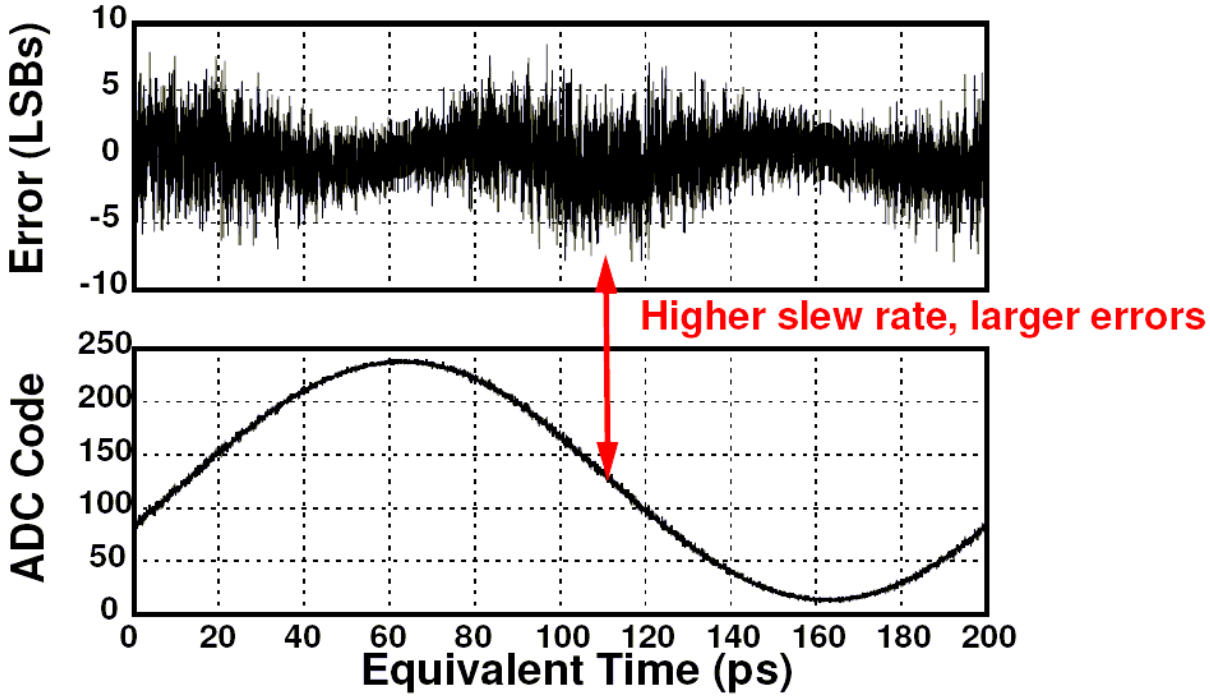
Fast input signal converts a sample timing error (dT) to an apparent voltage error (dV).



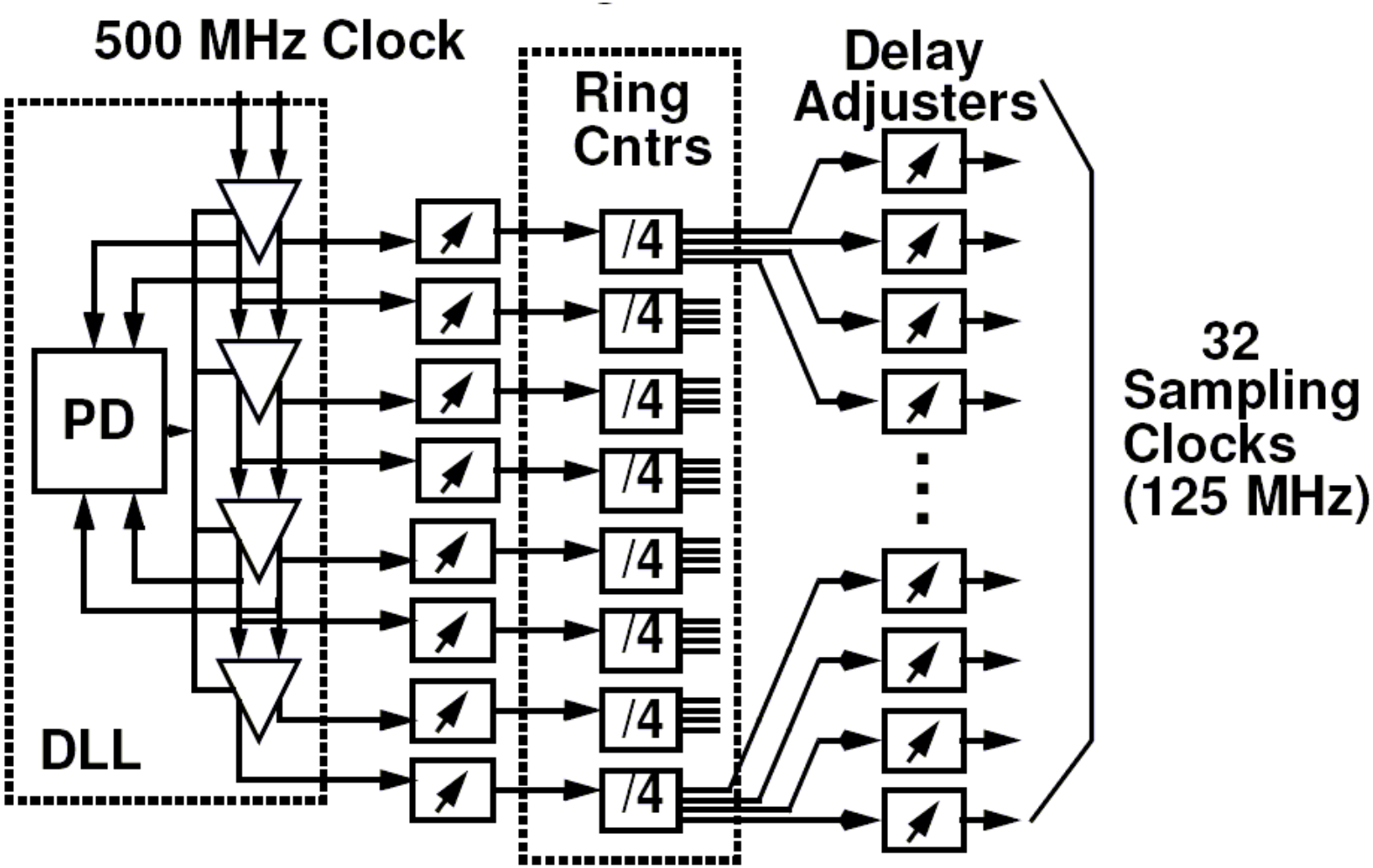
Rule of thumb:

1 ps @ 1 GHz -->

7 effective bits



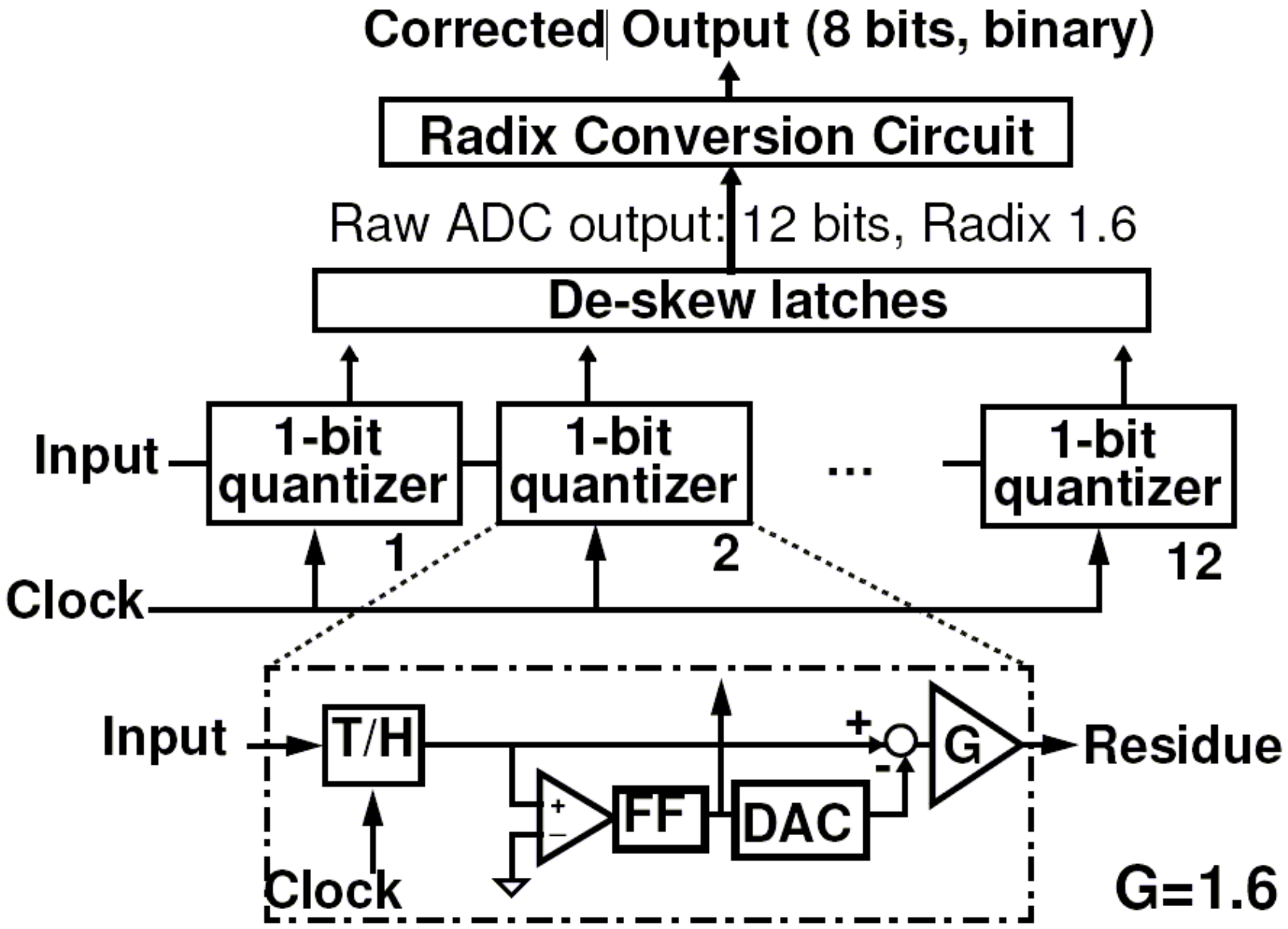
Timing Generator



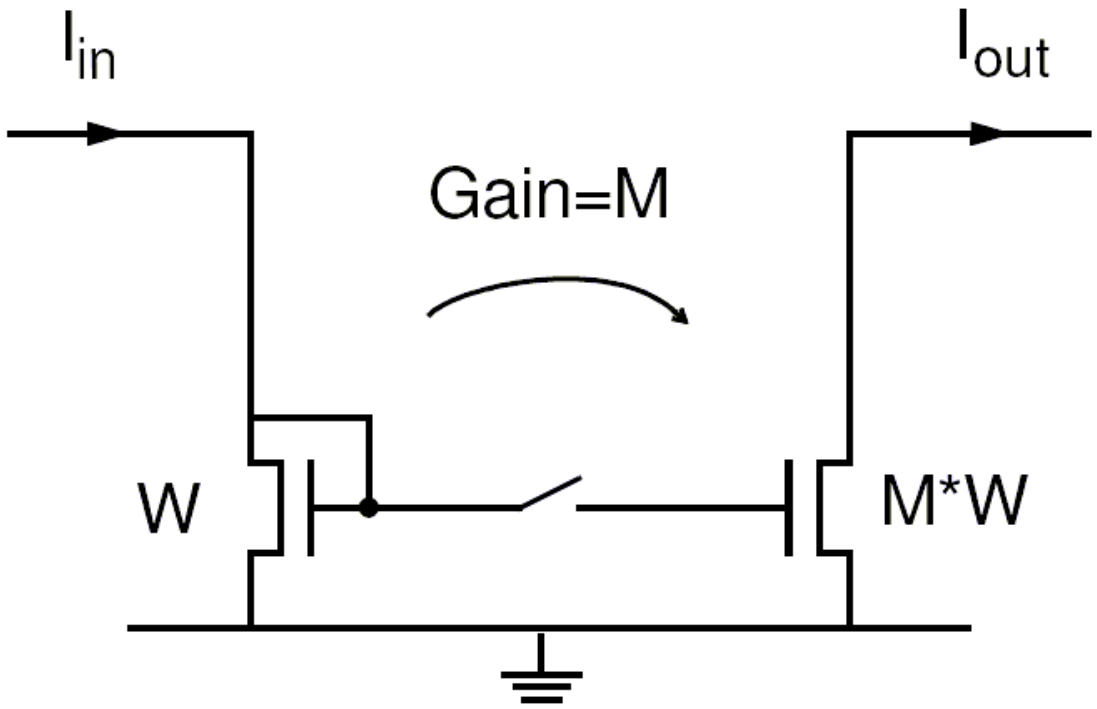
4 GSa/s: ~ 1 ps thermal jitter

Timing misalignments: before cal: 10 ps rms, after cal: 0.8 ps rms

Pipeline ADC Block Diagram



Current-Mode T/H and Amplifier



+ Fast: open loop amplifier

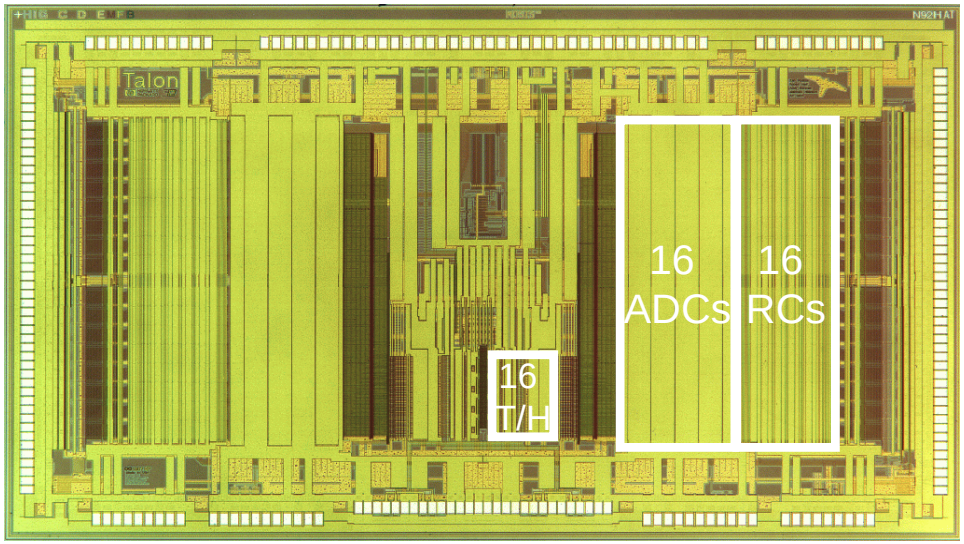
+ Good Linearity: Current mirrors with cascodes are 8 bit linear.

-- Poor Accuracy: Gain and offset errors

2002: 4-GSa/s 8-bit ADC

Compared to bipolar predecessor:

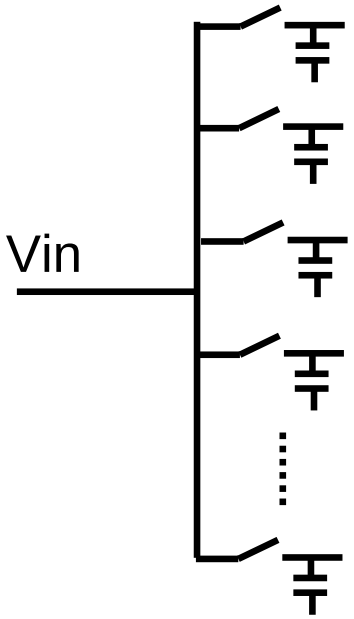
- same sample rate
- 100x more transistors
- + smaller area
- + 1 bit more resolution
- + better linearity
- -- 1.4x lower analog BW
- + 1/3 the power
- + 1/5 the cost



0.35-um CMOS
7.1 mm x 4.0 mm
300,000 FETs
4.6 W

Architecture: Coping With Wide Inputs

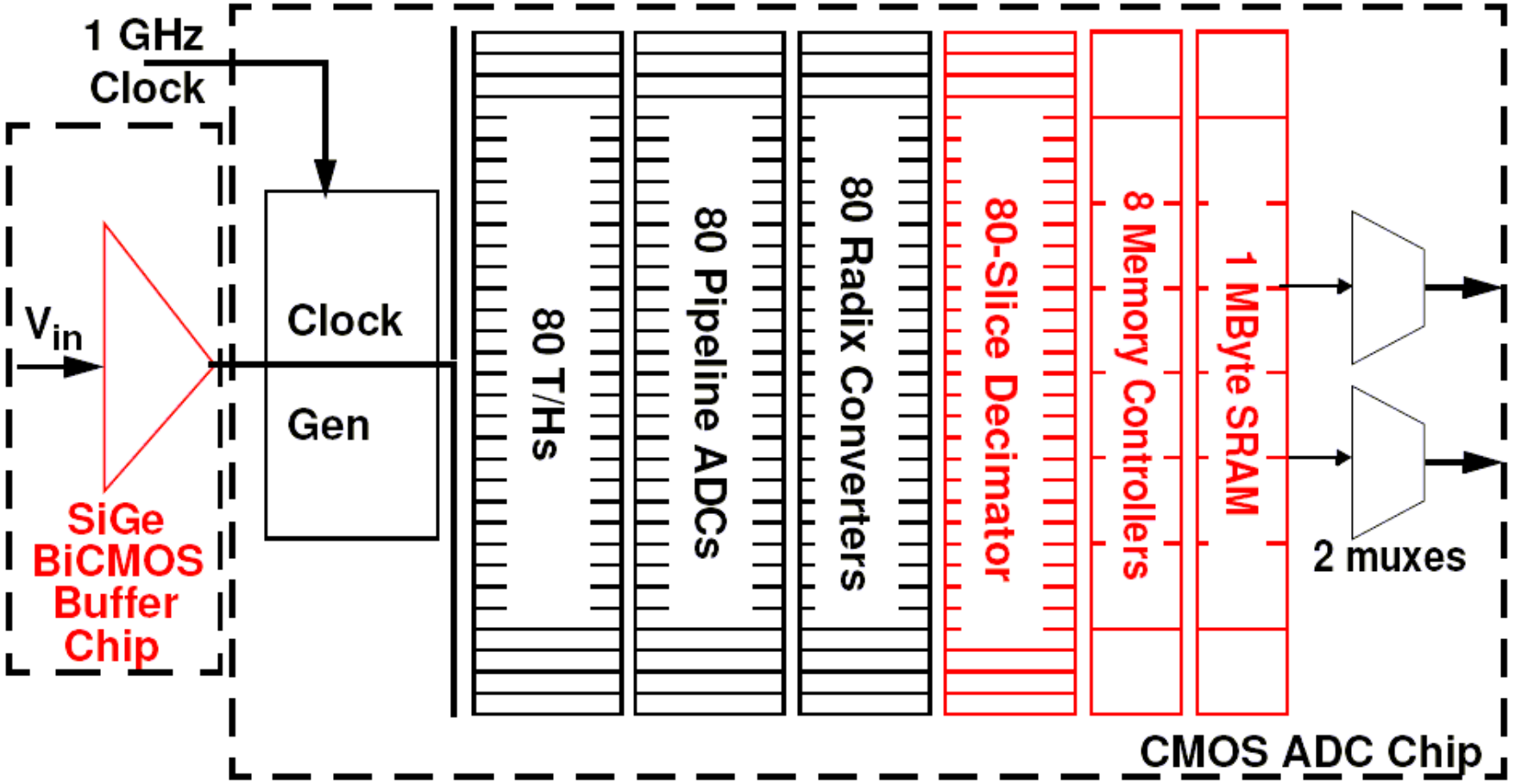
- Many parallel samplers connected to Vin cause:
  - High capacitance, e.g., 2 pF
  - Physical distribution challenges
    - Binary tree has matched lengths, but much more C
- Approaches:
  - Lower the input impedance
    - e.g., 25 ohms Rin
    - Add a buffer amplifier
  - Reduce the sampler count
    - One sampler feeds multiple ADC slices
    - Each sampler feeds multiple second-rank samplers



Architecture: Drinking From The Digital Firehose

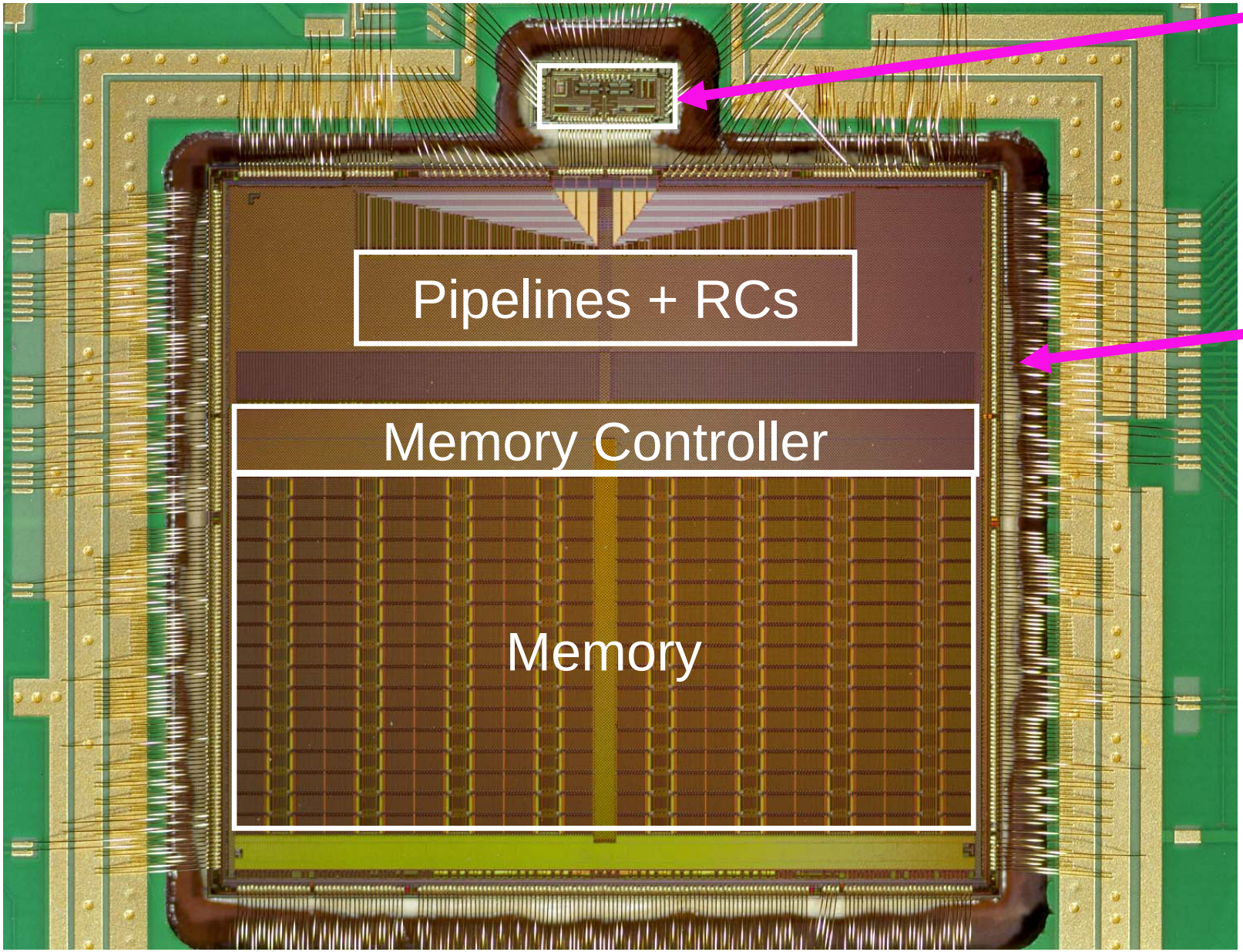
- Current gigasample ADCs spew out 4 to 500 Gb/s
- Parallel outputs – only 1-2 Gb/s/pair
- Serial outputs – 2-10 Gb/s/pair is now common.
  - FPGAs can catch this, but higher rates and pair counts can cost $1000 or more.
  - Dedicated data capture chips can catch 500 Gb/s, but it takes 50-100 lanes.
- On-chip storage – limited size; slow readout leads to ~90% deadtime
- On-chip processing – e.g., for communications receivers, can reduce the data rate by 2-10x for particular applications

2003: 20-GSa/s 8-bit ADC in 0.18 um CMOS



- 2x faster process, 5x higher sample rate, 6x higher BW
- 80 ADC slices, larger Cin --> SiGe input buffer chip
- 160 Gb/s data rate --> 1 MB on-chip sample memory

20 GSa/s ADC Module



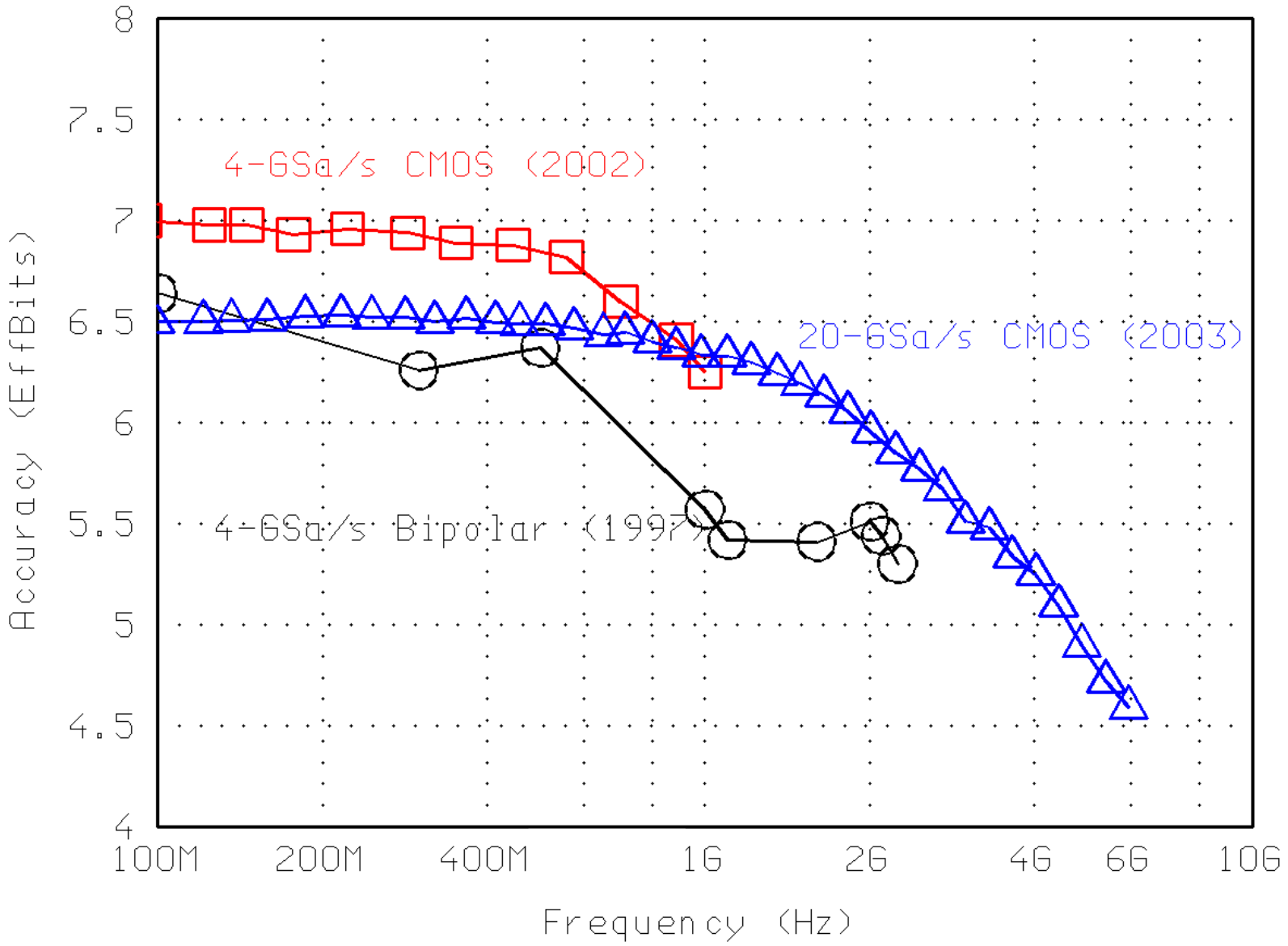
Buffer:
40 GHz SiGe
1 x 2 mm
1000 transistors
1 W

ADC:
0.18-um CMOS
14 x 14 mm
50M transistors
9 W

Package:
438-ball BGA
35 x 35 mm

Performance of Bipolar and CMOS ADCs

SNDR in Effective Bits



Architecture: Folding ADCs in CMOS

Venes & van de Plassche, “An **80-MHz**, 80-mW, 8-b CMOS Folding A/D Converter with Distributed Track-and-Hold Preprocessing”, ISSCC **1996**

- Brought the folding and interpolating architecture into CMOS
- 25x slower than HP’s 1997 bipolar folding ADC, 75x lower power

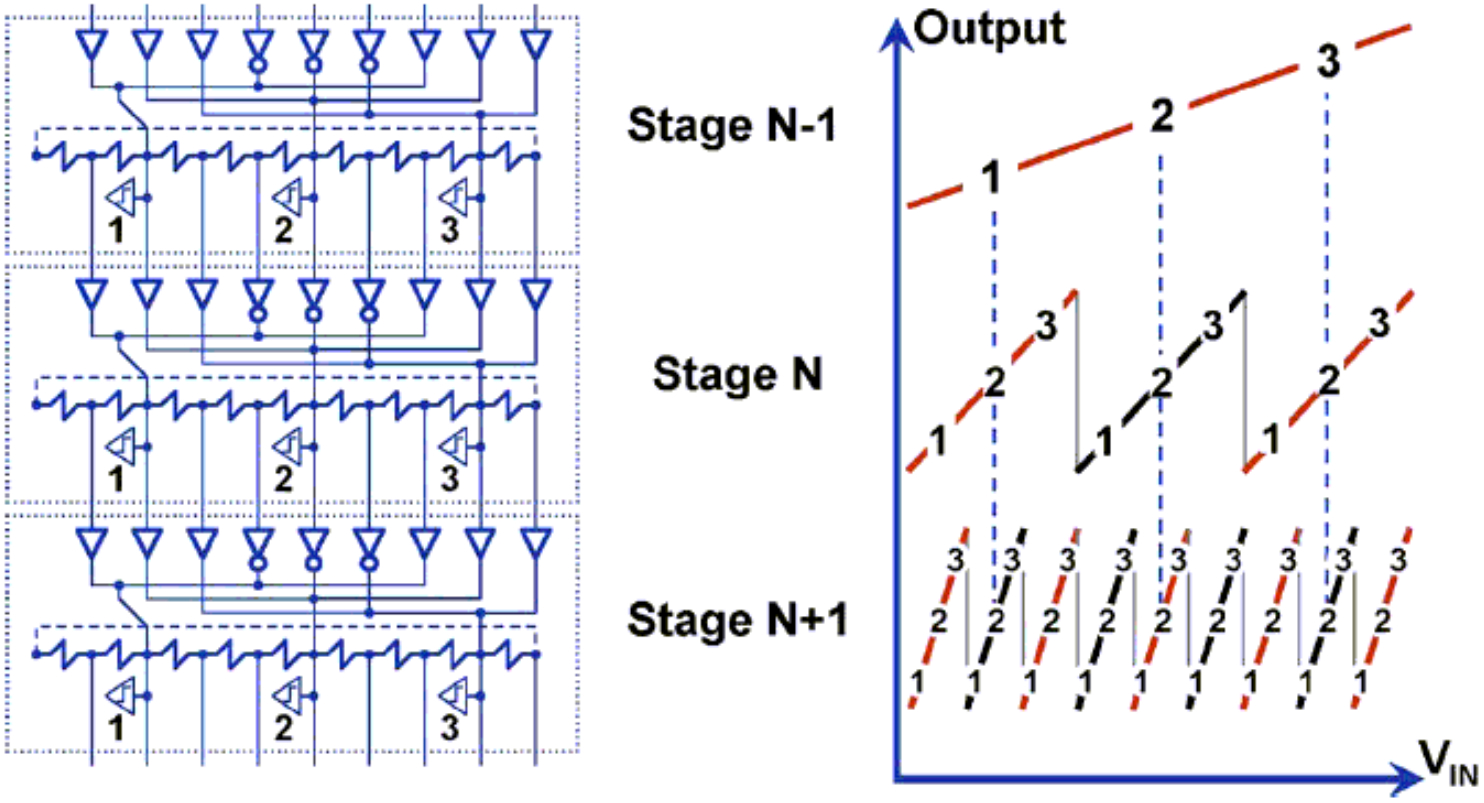
2008: CMOS folding ADCs reach the GSa/s range

- Lien & Lee, “A 6-b **1-GS/s** 30-mW ADC in 90-nm CMOS technology” A-SSCC **2008**
- Nakajima, et al, “A Background Self-Calibrated 6b **2.7 GS/s** ADC With Cascade-Calibrated Folding-Interpolating Architecture”, JSSC 2010
- Taft, et al, “A 1.8 V **1.0 GS/s** 10b Self-Calibrating Unified-Folding-Interpolating ADC With 9.1 ENOB at Nyquist Frequency”, JSSC 2009

Architecture: Cascaded Folding

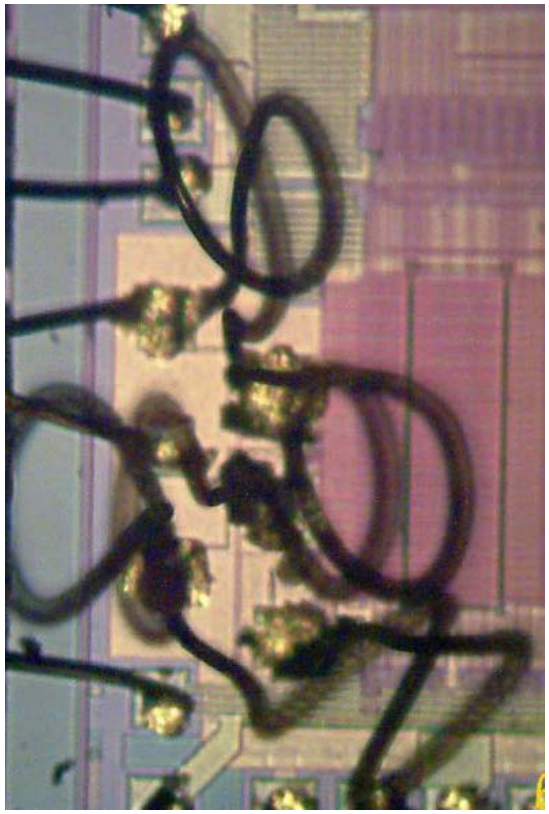
Taft, et al, “A 1.8 V 1.0 GS/s 10b Self-Calibrating Unified-Folding-Interpolating ADC With 9.1 ENOB at Nyquist Frequency”, JSSC 2009

- Cascaded folding stages 6 times to a total folding ratio of 729
- “MSB” comparators exist at each folding stage to avoid previous folding limits due to mismatch

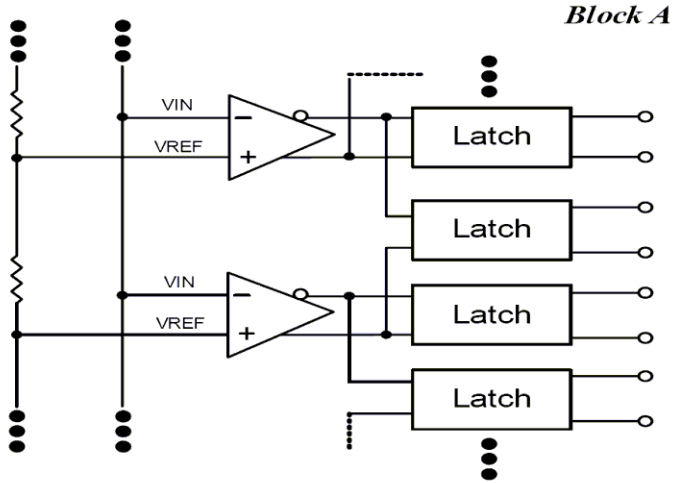


Architecture: Flash ADCs in CMOS

- Hero Projects
  - Walden, et al, “A 4-bit 1 GHz sub-half micrometer CMOS/SOS flash analog-to-digital converter using focused ion beam implants”, CICC **1988**
    - 5-V, 0.30-um CMOS using FIB lithography
  - Yang, et al, “A serial-link transceiver based on 8-GSamples/s A/D and D/A converters in 0.25-um CMOS”, ISSCC 2001
    - 4-bit, 1 GSa/s flash slices with bond-wire LC delay lines



- More Practical ADCs
  - Uyttenhove, Marques, Steyaert, “A 6-bit 1 GHz acquisition speed CMOS flash ADC with digital error correction”, CICC **2000**
  - Choi & Abidi, “A 6 b 1.3 GSample/s A/D converter in 0.35 um CMOS”, ISSCC 2001
  - Liang, et al , “10 GSamples/s, 4-bit, 1.2V, design-for-testability ADC and DAC in 0.13µm CMOS technology”, ASSCC 2007
  - Park, et al “A 6-bit 2GSPS **interpolated flash** type CMOS A/D converter with a buffered DC reference and one-zero detecting encoder”, NEWCAS 2005



Architecture: Interleaved Successive Approximation (SAR)

Chen & Brodersen, “A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-m CMOS”, JSSC 2006

- 2-way interleave of SAR slices with asyncronous cycle timing

Louwsma, et al, “A 1.35 GS/s, 10 b, 175 mW Time-Interleaved AD Converter in 0.13 um CMOS”, JSSC 2008

- 16-way interleaving of SAR slices

2008: Communications-focused ADCs

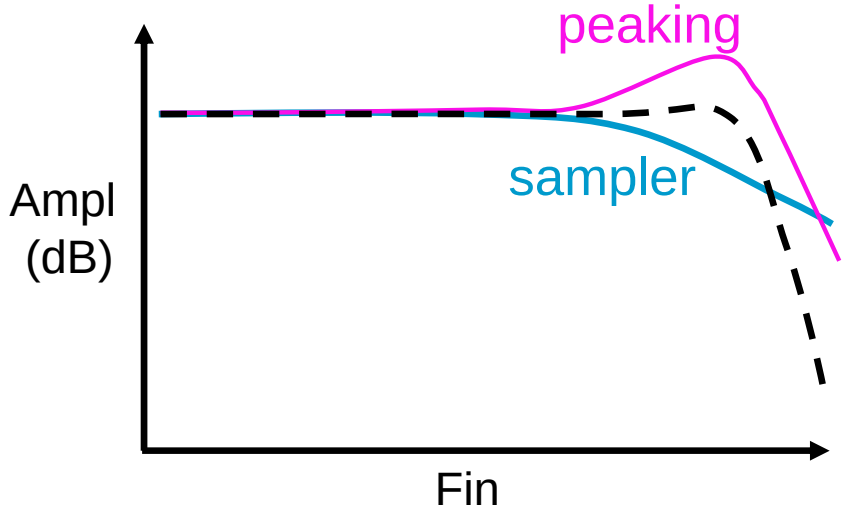
Schvan, et al, “A **24GS/s** 6b ADC in 90nm CMOS”, ISSCC 2008

- 160-way interleaving of 150 MSa/s SAR slice
- only 16 first-rank T/H’s at the input
- 4 effective bits at 12 GHz input
- Only 1.2 W

- Dedic, “**56Gs/s** ADC Enabling 100GbE”, OFC 2010
  - 56 GSa/s, 8 bits, aimed at 28 Gb/s line rate
  - 320-way interleave of 175 MSa/s SAR slice
  - “Charge Mode Interleaved Sampler” is named, but not described
  - 5.5 effective bits at 15 GHz input is quite good
  - 2 W in 65 nm

Architectures for Extending Bandwidths

Sample rate is extensible by more interleaving, but bandwidth is not so simple.



Analog peaking

+ extend the BW of an input sampler

-- hard to align over process, temperature

-- can only work where the analog loss is small

-- amplifies preamp noise in the boost region

Digital peaking

• implemented after the ADC

• same plusses and minuses, plus

+ avoids analog circuit development

-- amplifies quantization noise in the boost region

More Architectures for Extending Bandwidths

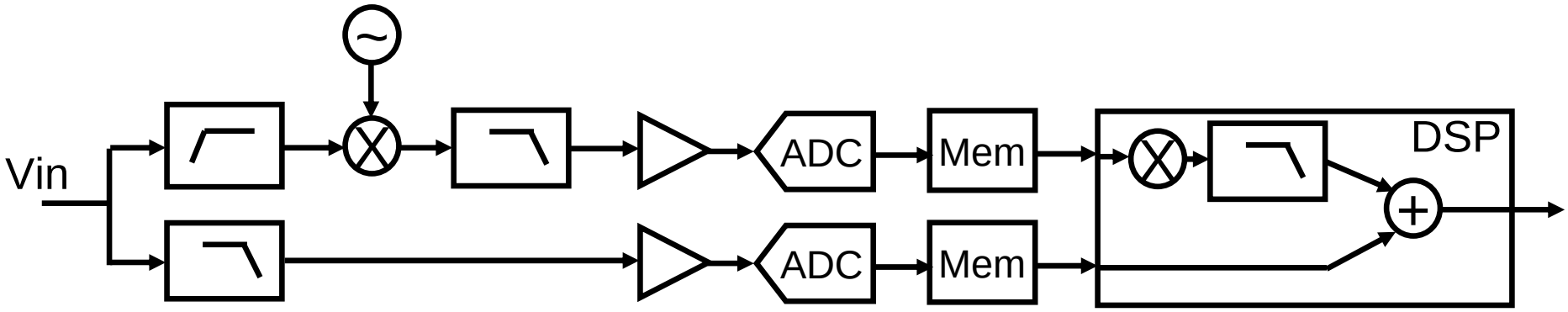
Frequency Interleaving

- Filter the input signal into lower and upper bands (e.g, 0-10 and 10-20 GHz)
- Mix upper band (e.g., 10-20 GHz) down to baseband
- Digitize each band at baseband, e.g., at 25 GSa/s
- After the ADC, use DSP to mix upper back up and combine with the lower band
- Apply lots of flatness and phase corrections

\+ Mixers are cheaper than doubling ADC BW

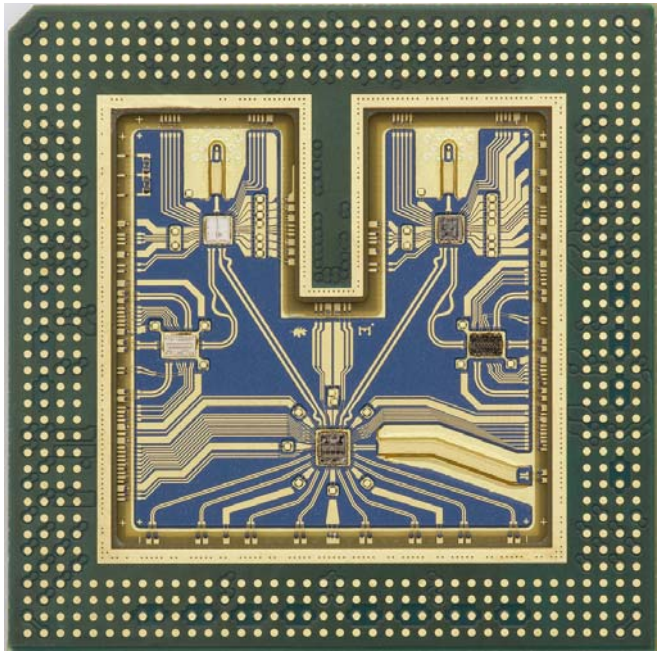
-- Hard to align band edges over process, temperature

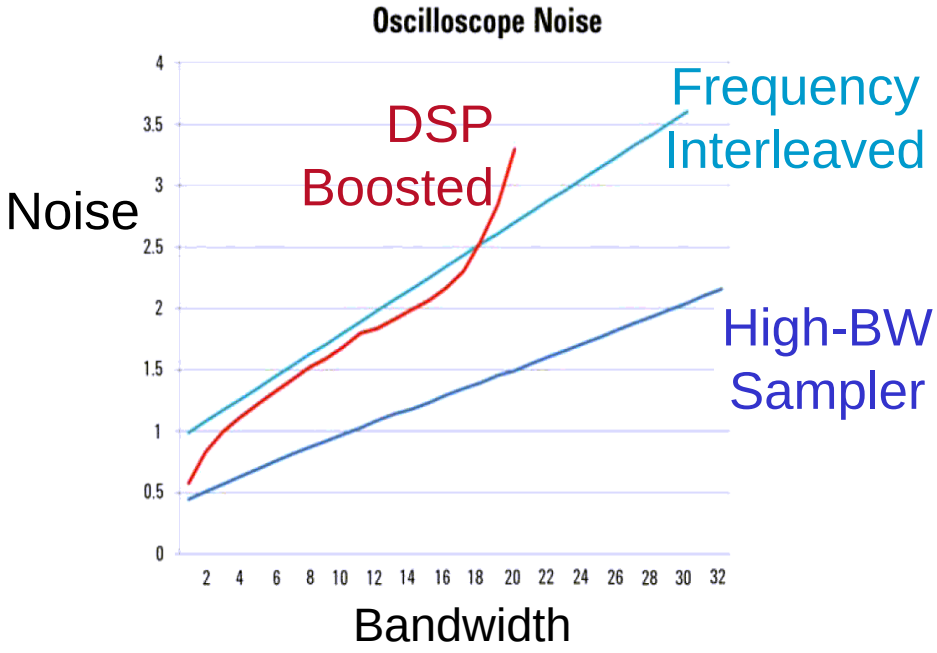
-- Noisy



2010: 80 GSa/s, 32 GHz BW

- Sampler in 250 GHz InP HBT process
  - 32 GHz native analog BW
- Drives four CMOS ADC chips
  - 80 GSa/s
- 5-chip module
  - avoids 32 GHz interconnects on PCB
- Noise ~2x lower than other methods





- For details see the upcoming paper at CSICS in October:

  Shimon, et al, “InP IC Technology Powers Agilent’s 90000X Series Real Time Oscilloscope Family”, CSICS 2010

Trends

Processes

- CMOS has mostly taken over ADC chips, even at the highest sample rates
- Bipolar circuits have a place in some high-BW front ends
- VDD scaling has stalled near 1 V in recent generations of digital CMOS
    - 1-V analog design is becoming more mainstream
    - Analog can now utilize the huge raw speeds of recent CMOS

Architectures

- Gigasample ADCs rely on both innovation and recycling of old ideas
- Massive time interleaving is key to the highest sample rates
- Most known ADC architectures now find some use in gigasample ADCs

Markets

- Optical communications is now driving the highest speed ADCs
- Multilevel signaling at 5-10 Gbaud/s may become another ADC driver

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(end)