# Building the World's Fastest 8-bit ADC - In CMOS

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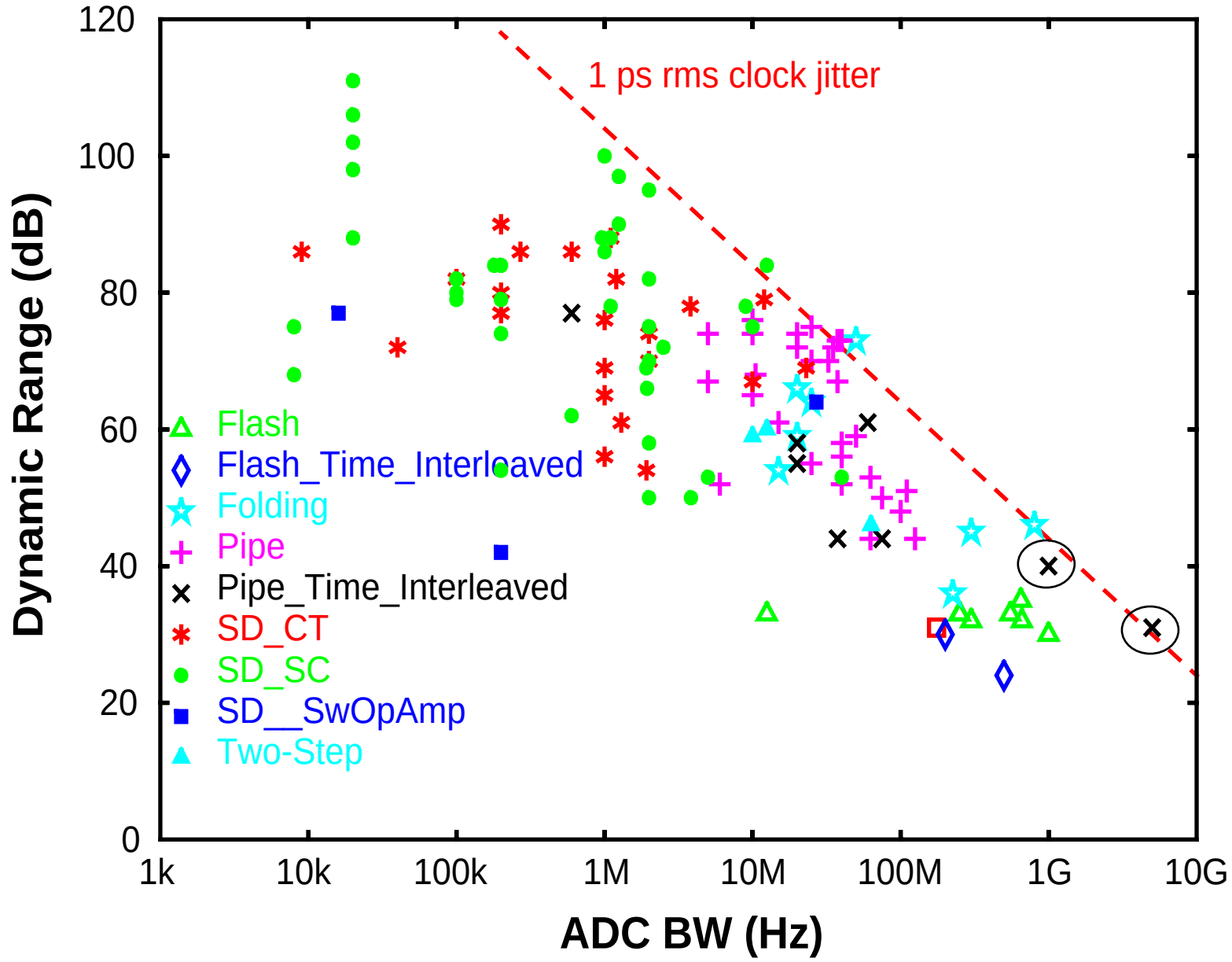
# Outline

- Trends in CMOS ADCs
- Massively Interleaved ADCs
  - 4 GSa/s
  - 20 GSa/s

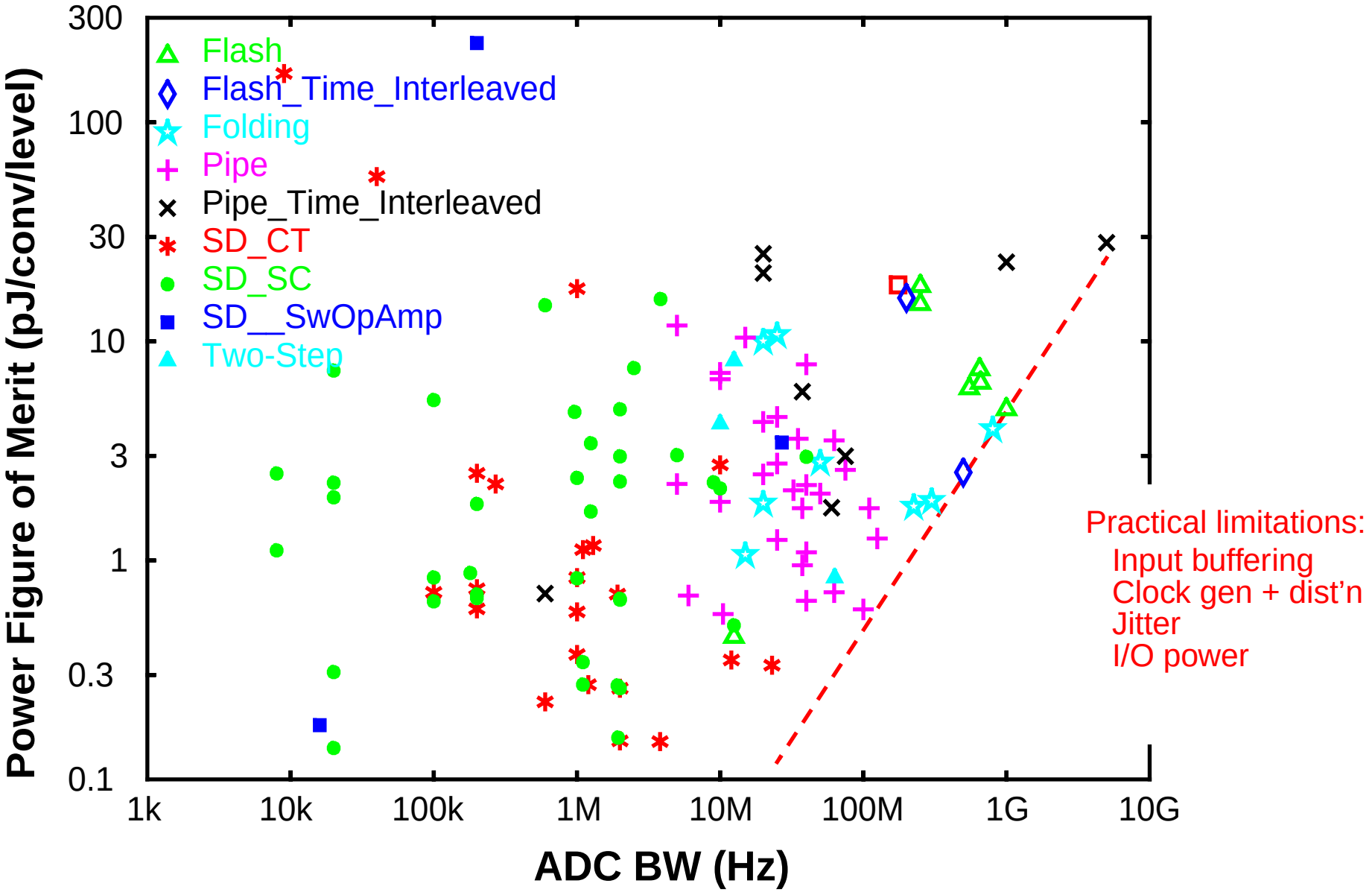
# ADC Dynamic Range vs. Input BW - ISSCC 1998-2005




Data courtesy of Boris Murmann

# ADC Figure of Merit vs. Input BW - ISSCC 1998-2005

$$FOM = P / ( 2^{ENOB} * 2 * F_{IN})$$



# Some Trends in CMOS ADCs

- Increasing focus on power reduction
  - Battery-powered (e.g., toys, laptops) - supply limited
  - High-end ADCs (e.g., scopes) - dissipation limited
  - System-on-a-Chip (e.g., wireless, PDAs) - can have both limits
- Increasing numbers of embedded ADCs and DACs
- Lower-voltage CMOS tends to take *more* power to maintain the same SNR
  - ➪ Increased advantage in replacing analog functions with digital
- Lower-voltage CMOS makes precision analog circuits harder
  - ➪ Increasing use of simpler analog circuits
  - ➪ Increasing use of digital techniques to address analog imperfections
- Calibration Techniques
  - Foreground calibration used in some ADCs
  - Background calibration starting to move beyond academic ADCs

# Process Selection

*Poulton's Polemic:*

"Don't use III-V FETs if HBTs will work.
Don't use III-V HBTs if silicon will work.
Don't use bipolar if CMOS will work."

*Robertson's Reason:*

"If we don't do it in CMOS, someone else will."

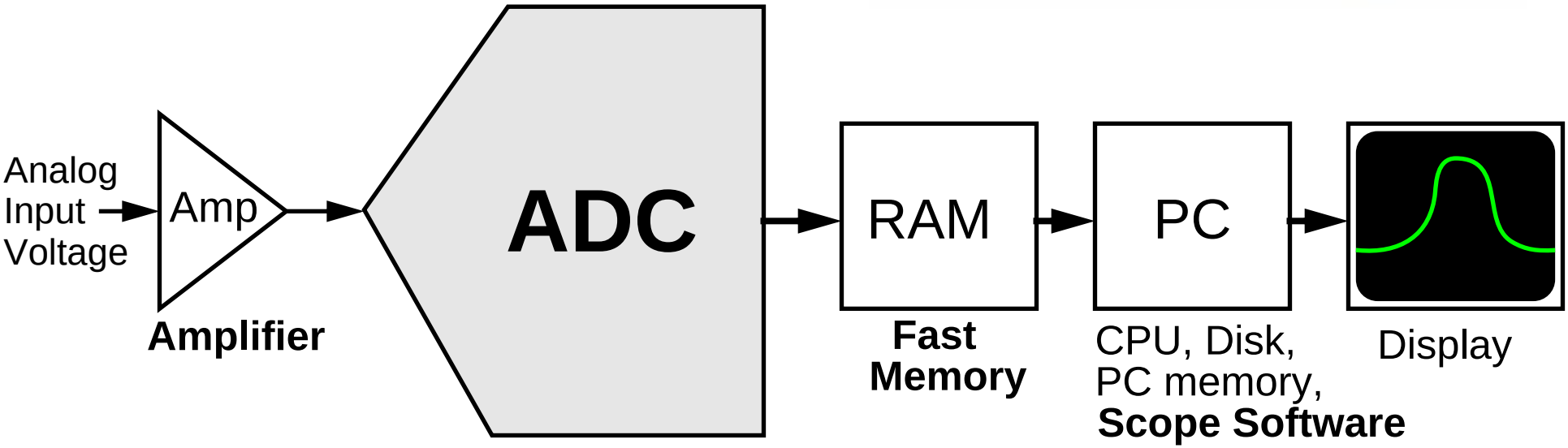
- CMOS is cheaper (at least in volume)
- CMOS circuits are more widely reusable
- CMOS designers are less difficult to hire

- But some jobs do need other technologies

# What's in a Scope?

The Scope User's View:

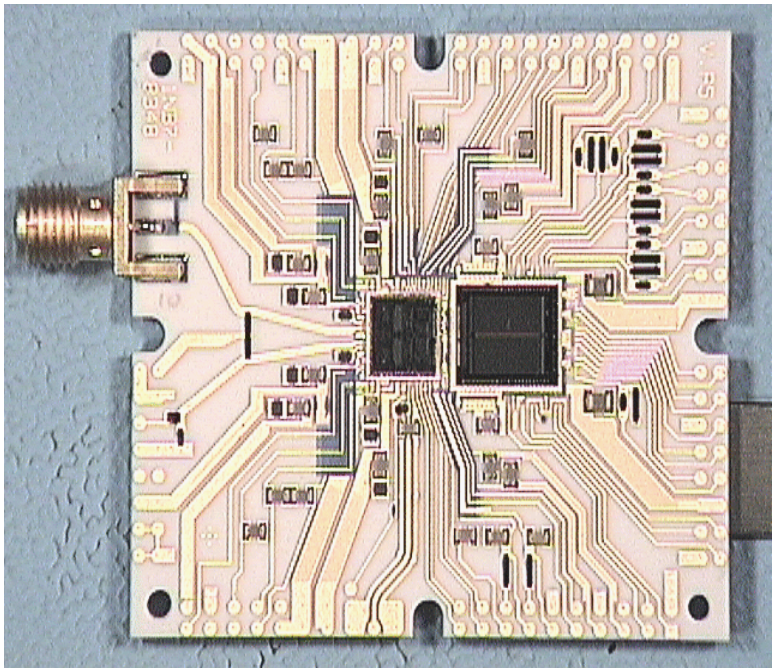
The ADC Designer's View:




- Resolution - 8 bits
- Realtime BW up to $F_S/2.5$
- Money specs: bandwidth and sample rate

# Designing Scope ADCs the Old Way

- Approach:
  - Use the fastest technology available
  - Design for the highest sample rate
  - If necessary, time-interleave 2-6x
- State of the Art in 1996:
  - 25-GHz bipolar process
  - 2-GSa/s unit ADC
  - Interleaved 2x to get 4 GSa/s on one chip
  - 2.2 GHz BW (with 4x interleave)
  - 6.5 effective bits at 100 MHz
  - 5.4 effective bits at 1 GHz
  - 13 watts
  - Expensive



**Custom thick-film package with custom bipolar ADC chip and custom CMOS memory chip**

# Could We Use CMOS for Scope ADCs?

"Don't be stupid:"

- CMOS ADCs are 60 times too slow (in 1996)
- CMOS transistors are 10 times less accurate than bipolars

"But..."

- CMOS chips are cheap and transistors are virtually free
- Could integrate with memory
- Might be lower power
- One high-BW circuit: the NMOS track-and-hold (T/H)

# Idea: Massive Interleaving of Low-Power ADCs

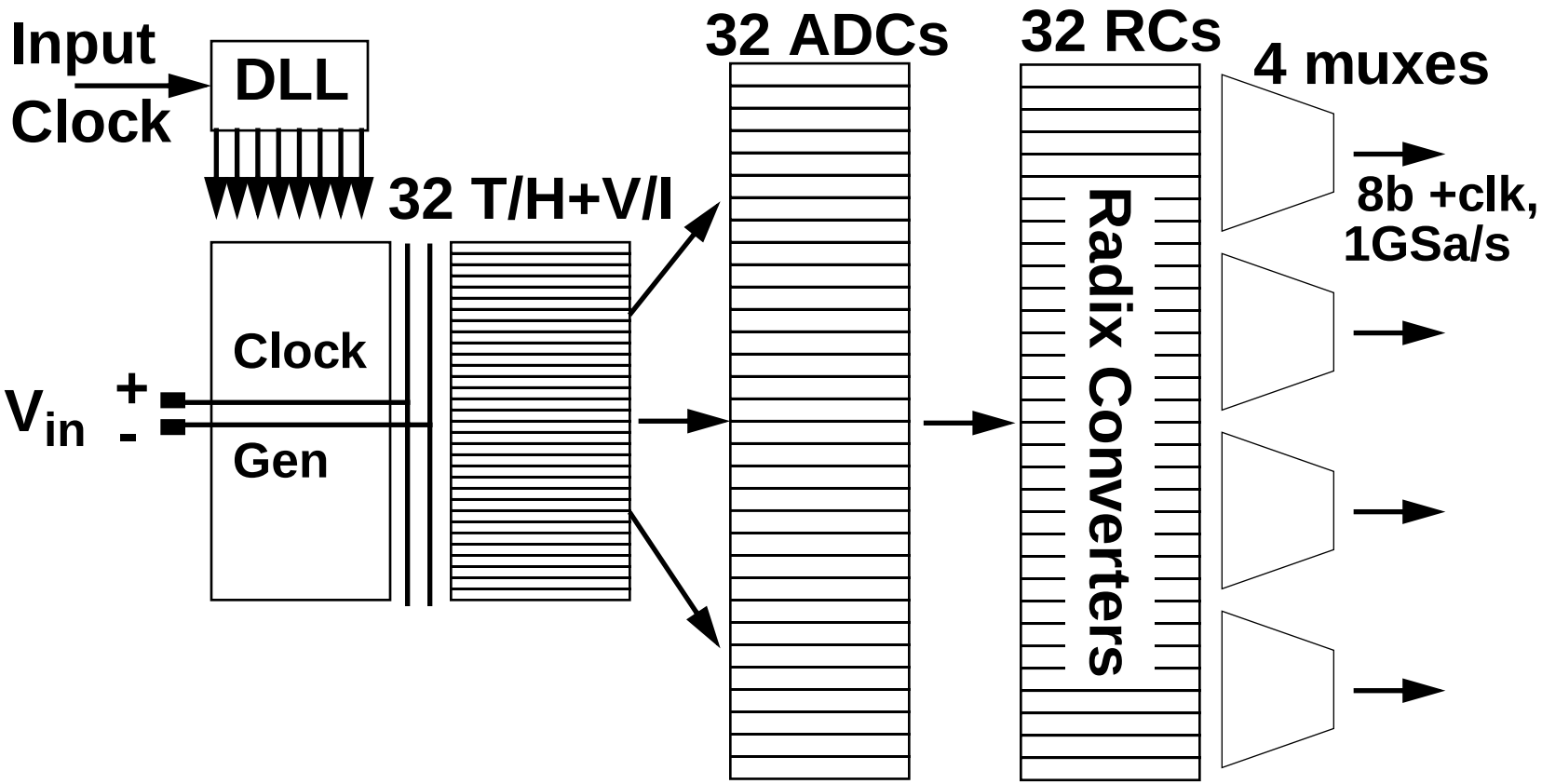
- Start with the most power-efficient CMOS ADC slice
- Time-interleave like crazy to get sample rate
- Fix up analog accuracy through calibration

Challenges:

Track/Hold : Bandwidth, Channel mismatch, Clocks

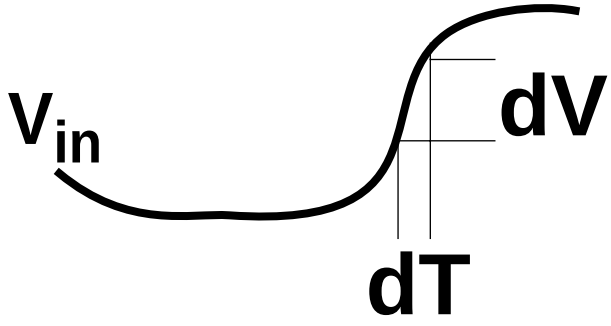
ADC: Sample Rate, Power/sample, Circuit area

# CMOS ADC Chip Architecture (4 GSa/s)

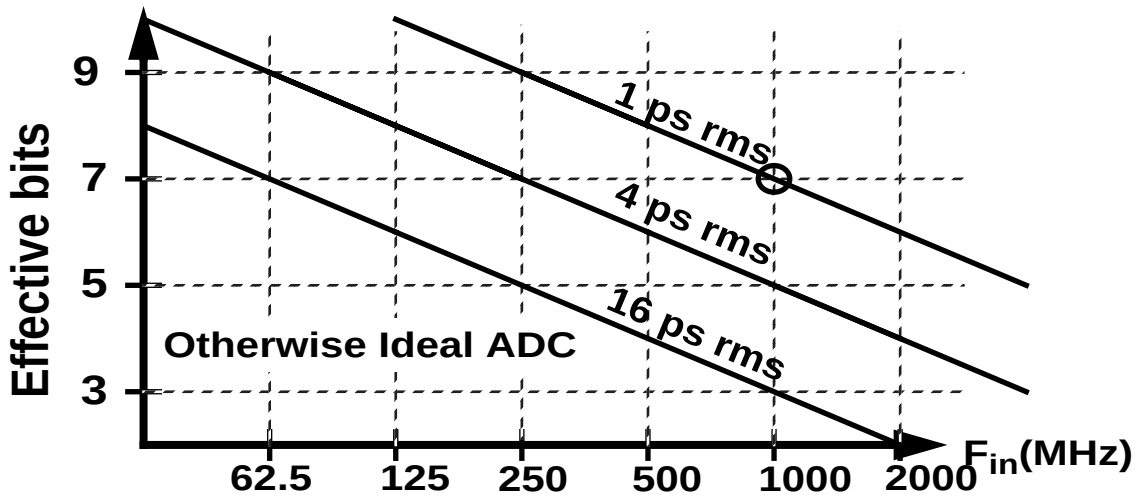



- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s

# Timing Error and ADC Resolution

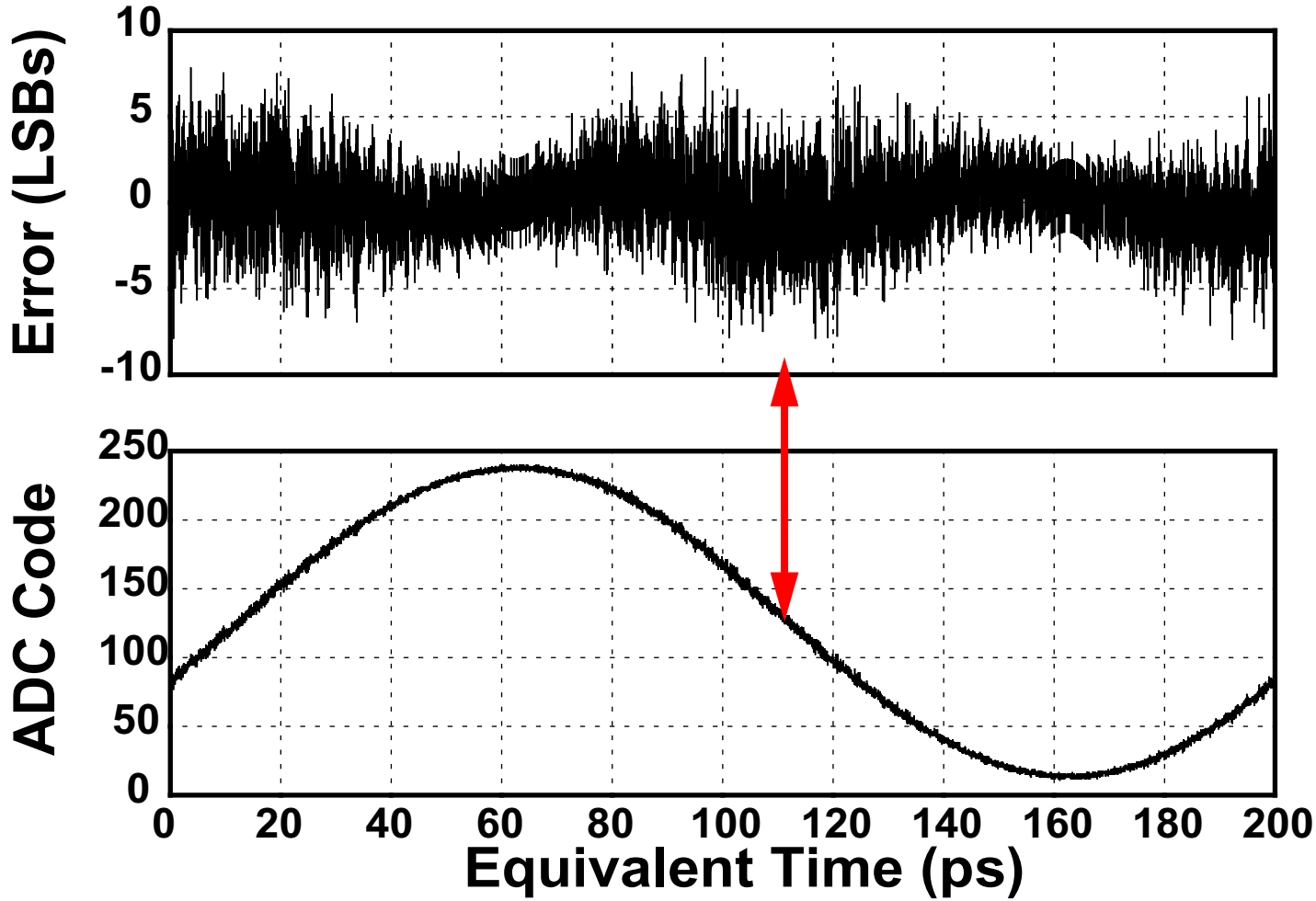



- Fast signal converts a sample timing error (dT) to an apparent voltage error (dV).




- Rule of thumb: 1 ps / 1 GHz --> 7 effective bits

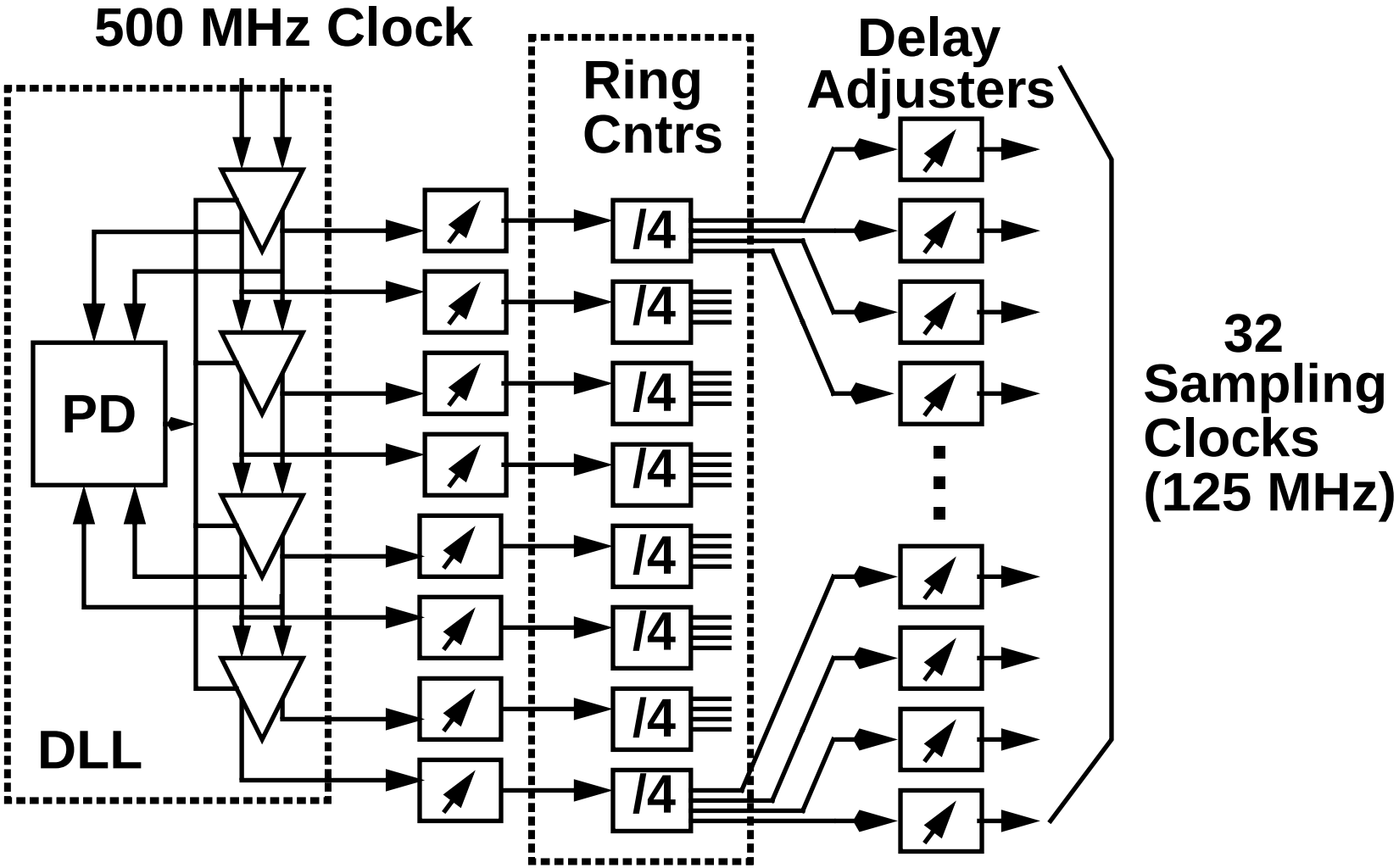
# Timing Error Signature




- Larger voltage errors during high dV/dt.

  Fs = 20 GSa/s  Fin = 5007.5 MHz  5.0 effective bits

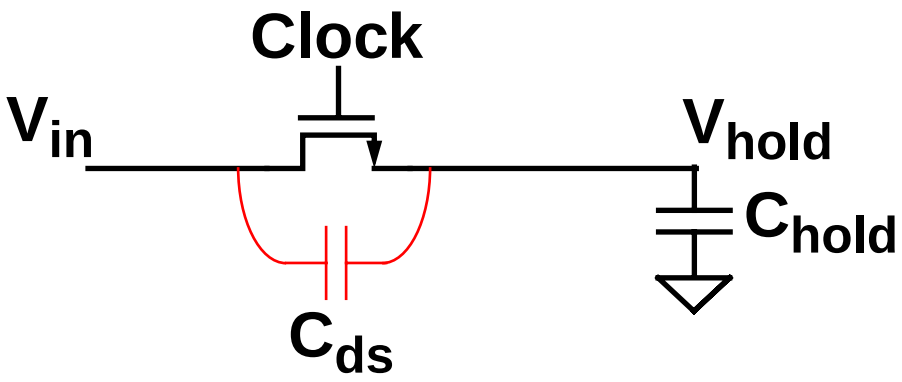
# Timing Generator




- Max input edge to sampling edge delay: 2 ns

  **~ 1 ps jitter** **< 1 ps static error after cal**

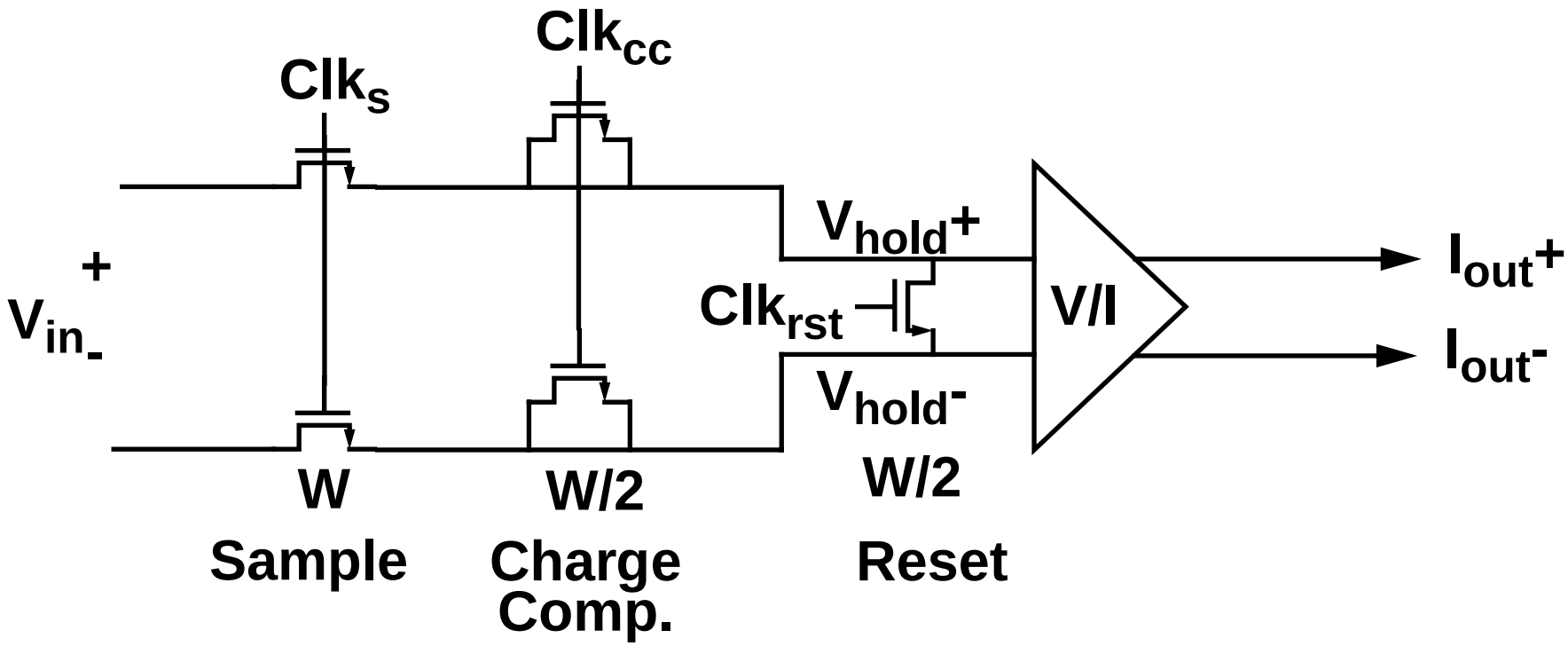
# Simplified Input Track/Hold




- To achieve highest bandwidth and linearity:
  - ***ONLY*** 1 NMOS FET in signal path
  - Restrict $C_{hold}$ to only T/H and load parasitics
  - Low common mode input voltage
  - Low-swing differential signal (250 mV peak)
  - Fastest possible full-swing clock edge

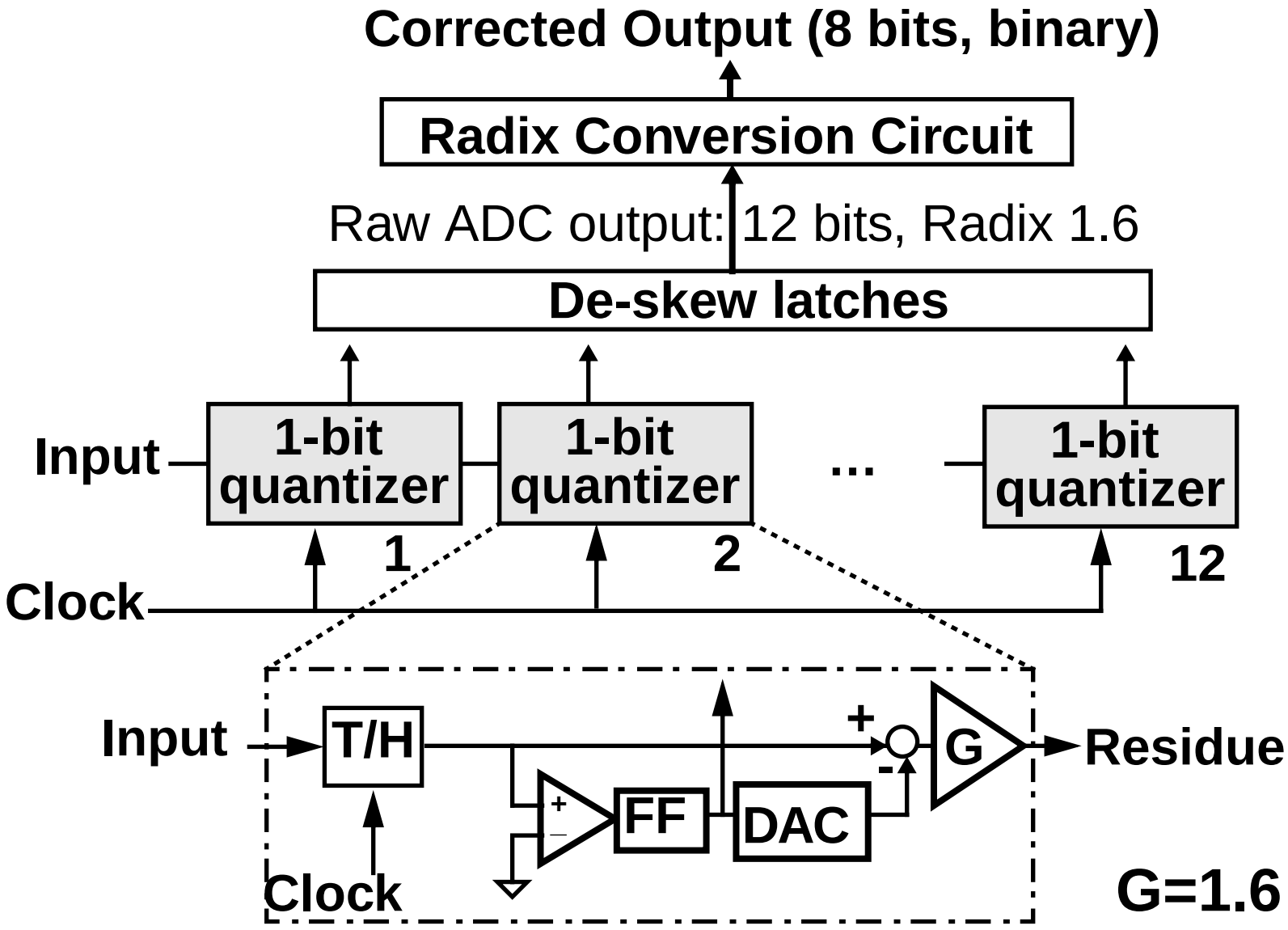
In 0.35 um: 2 GHz bandwidth, -50 dB HD3
In 0.18 um: 7 GHz bandwidth, -50 dB HD3

# Analog Front End Implementation



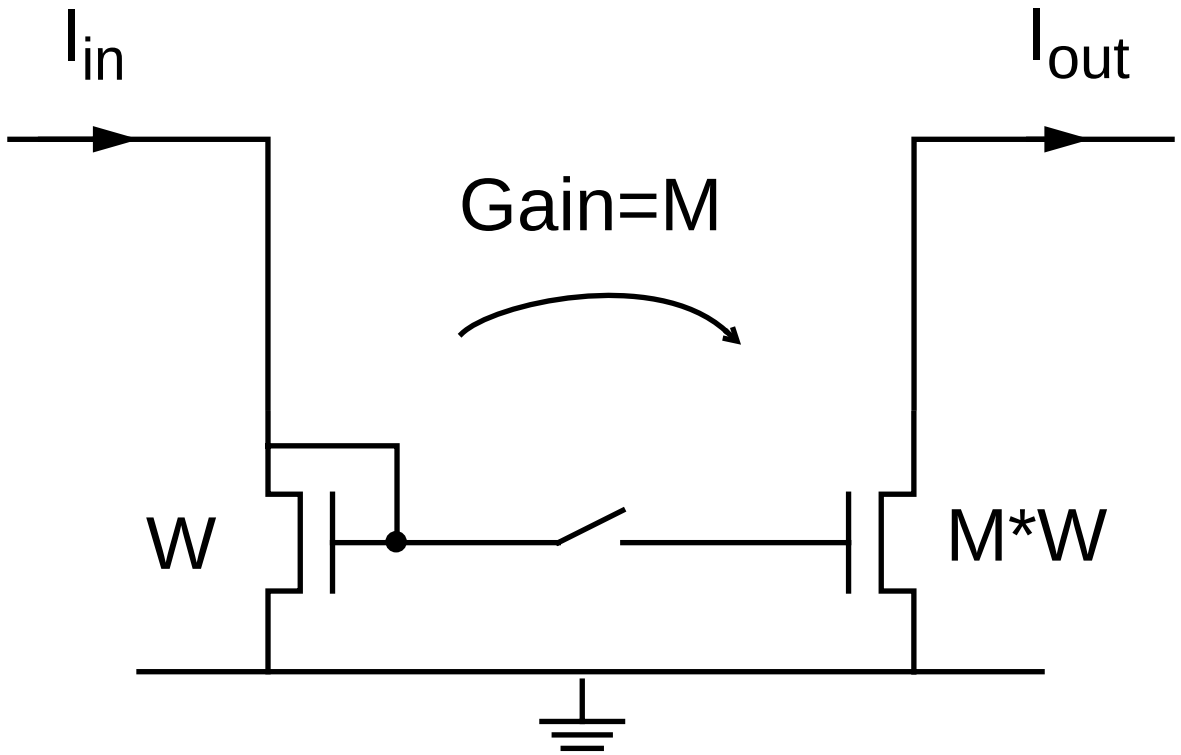

- Parasitic-only hold capacitance (140 fF)
- Only 1 ns (12.5%) pulse width for $Clk_s$
- Reset phase
- Transconductor (V/I) current output drives ADC

# Pipeline ADC Block Diagram




- Only 1 comparator per stage

# Current-Mode T/H and Gain




- Good Linearity: Current mirrors with cascodes are 8 bit linear.
- Poor Accuracy: Gain and offset errors

# Radix Converter Principle

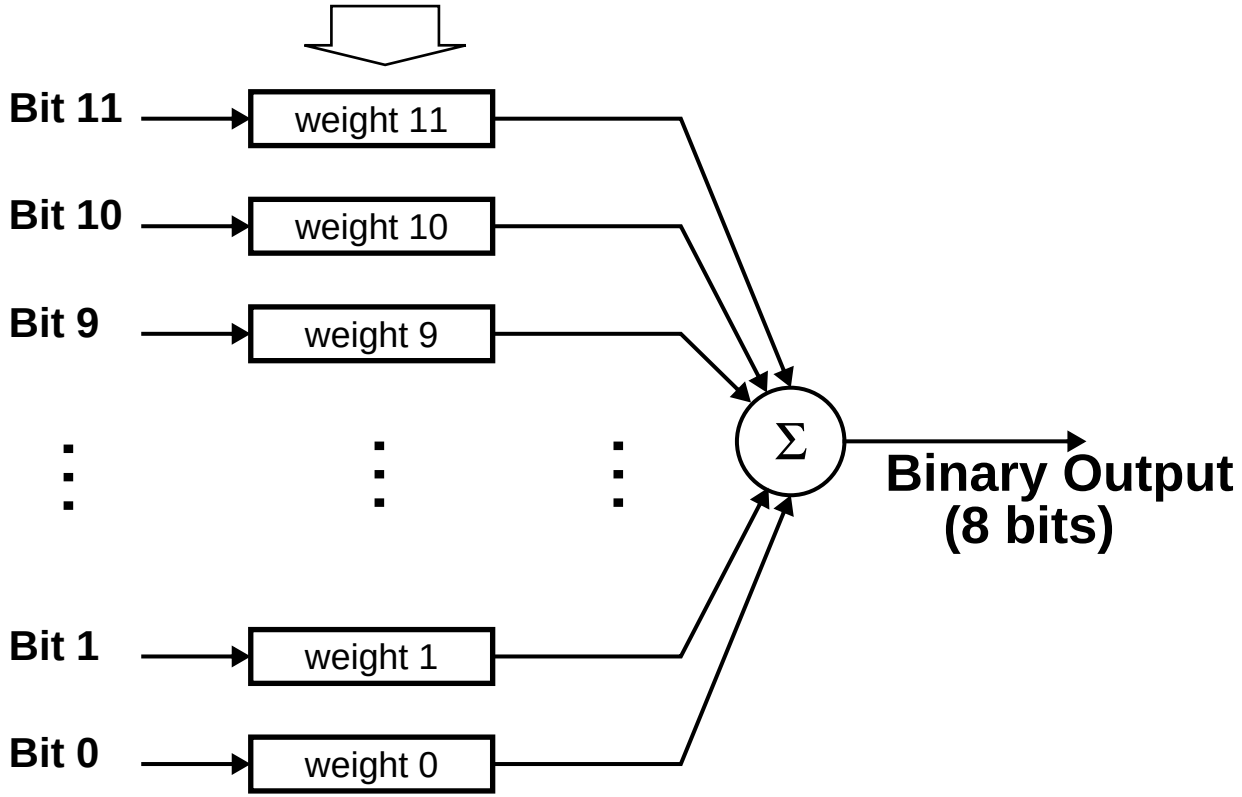
- ADC is performing linear operations.
- Output bits are can be linearly combined to represent input signal:

  **ADC output = $b_{11}.w_{11} + b_{10}.w_{10} + \ ... \ + b_1.w_1 + b_0.w_0$**

- Traditional design: Accurate analog design
  - $w_i$ are powers of 2
  - No explicit Multiply/Accumulate needed.
- Digital Calibration:  Approximate analog design.
  - Actual $w_i$ are measured through calibration
  - Compliments reduced radix approach.
  - Requires Multiply/Accumulate block.

# Multiply/Accumulate (Radix Converter)

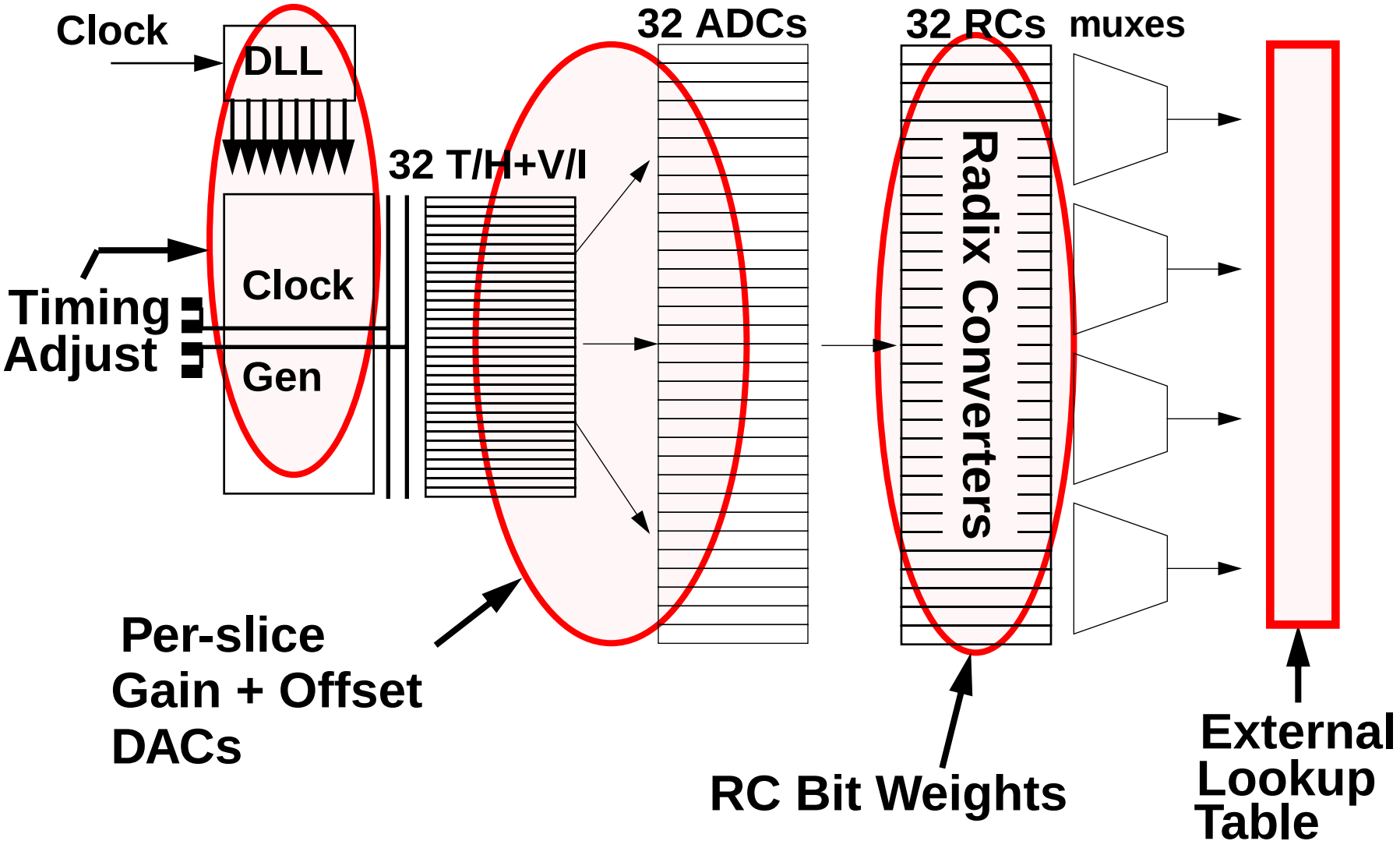
**Calculate and download bit weights during cal.**




$$\text{Output} = b_{11}.w_{11} + b_{10}.w_{10} + \ldots + b_1.w_1 + b_0.w_0$$

- 1 bit “Multiply” is just a memory access
- Look-up table is an alternative.

# What Needs To Be Calibrated?

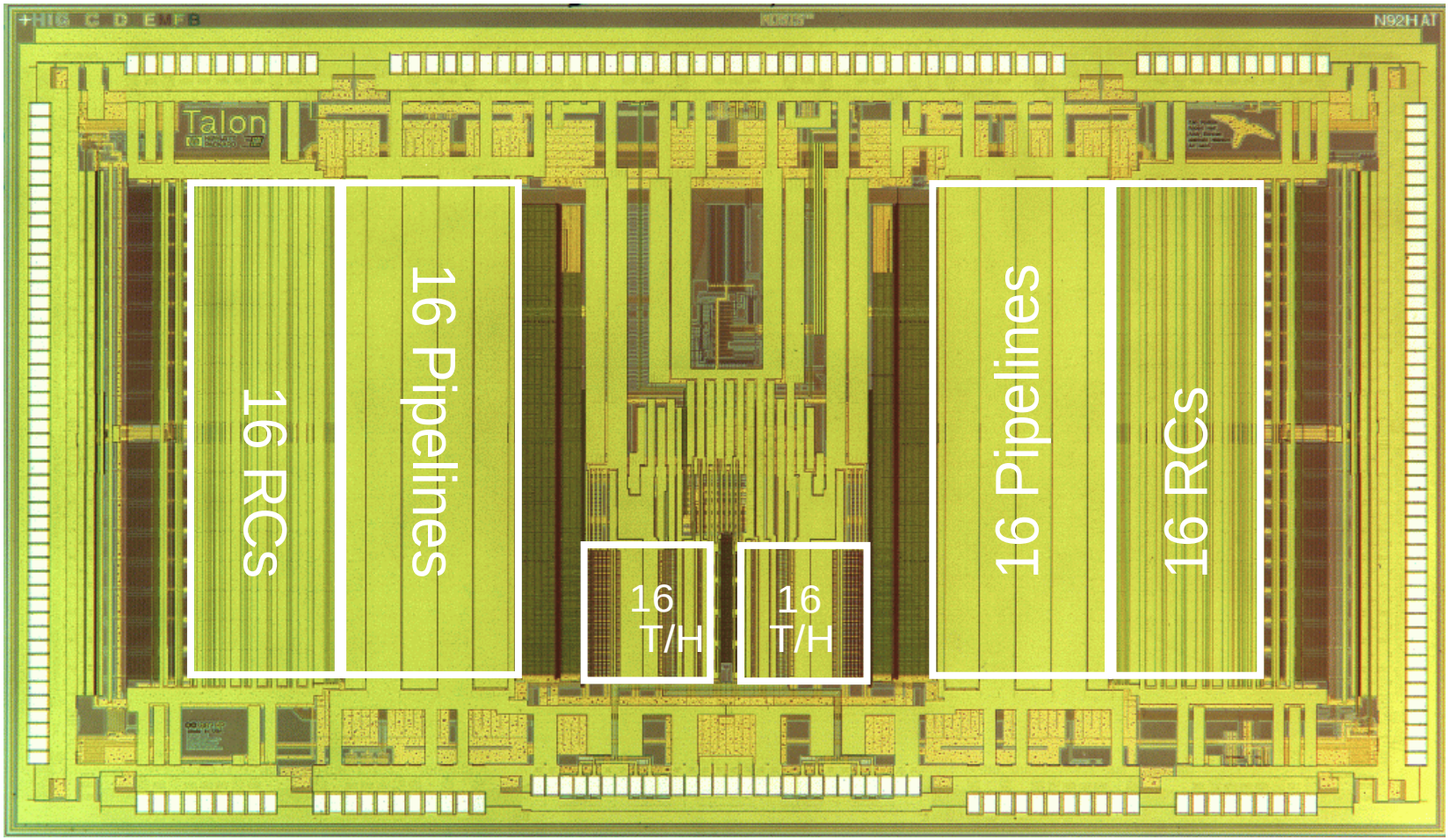



- Offline Calibration with DC and Pulse sources

# Advantages of a Calibration Approach

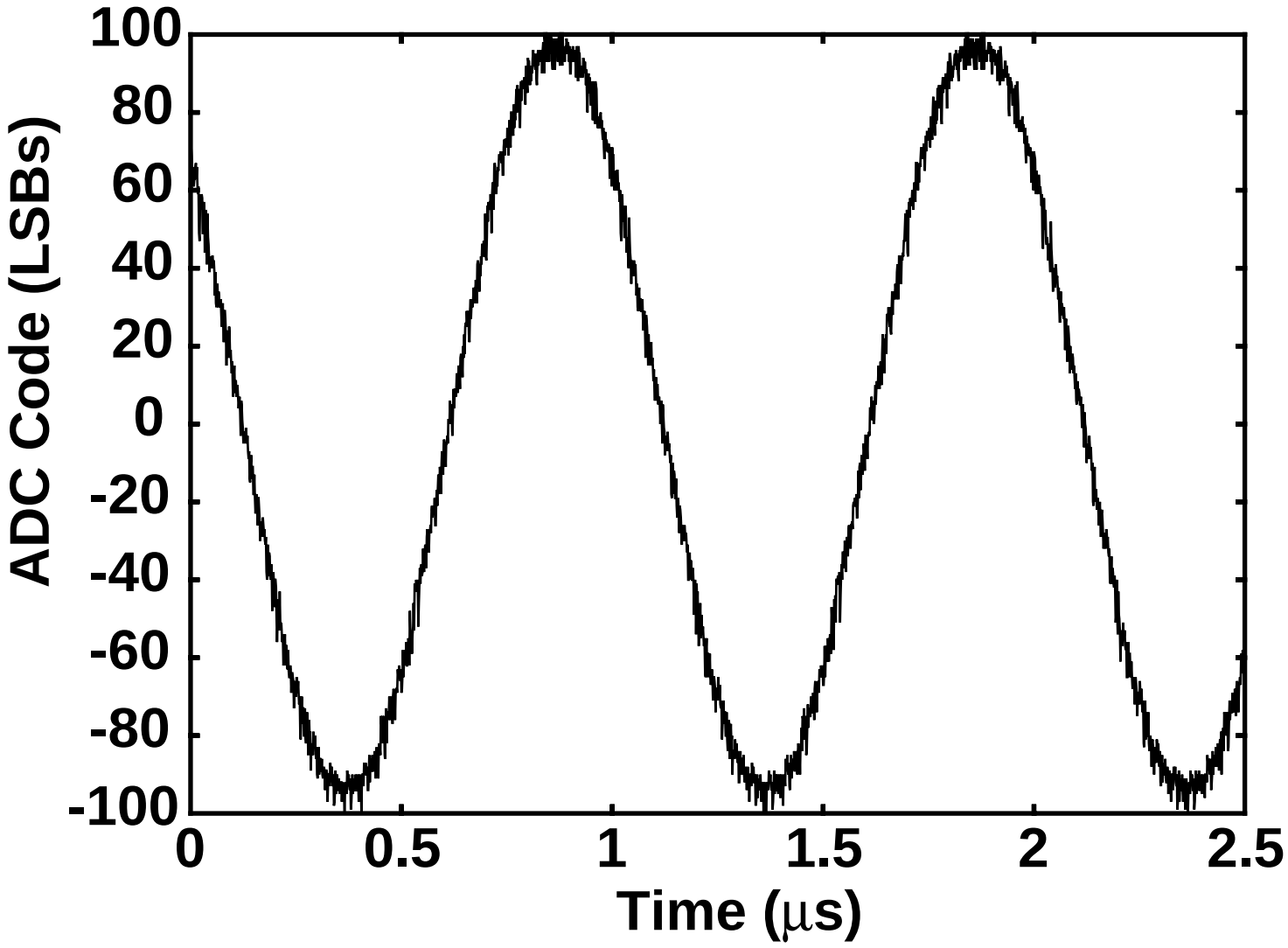
- We can get away with approximate analog design.
  - No 6-sigma 1% matching needed in ADC slice.
  - Do not need precise modelling of 2nd order mismatch effects (like layout related delta W).
  - Time delay mismatch can be tolerated.
  - Signal path offset and gain errors are easily cal'ed.
  - If an effect can be calibrated, and a reasonable bound on its effect computed, then design of the calibration DAC is relatively simple.
- Benefits:
  - Reduced design time.
  - High yield possible with many ADCs / chip.

# 4 GSa/sec ADC Chip Layout



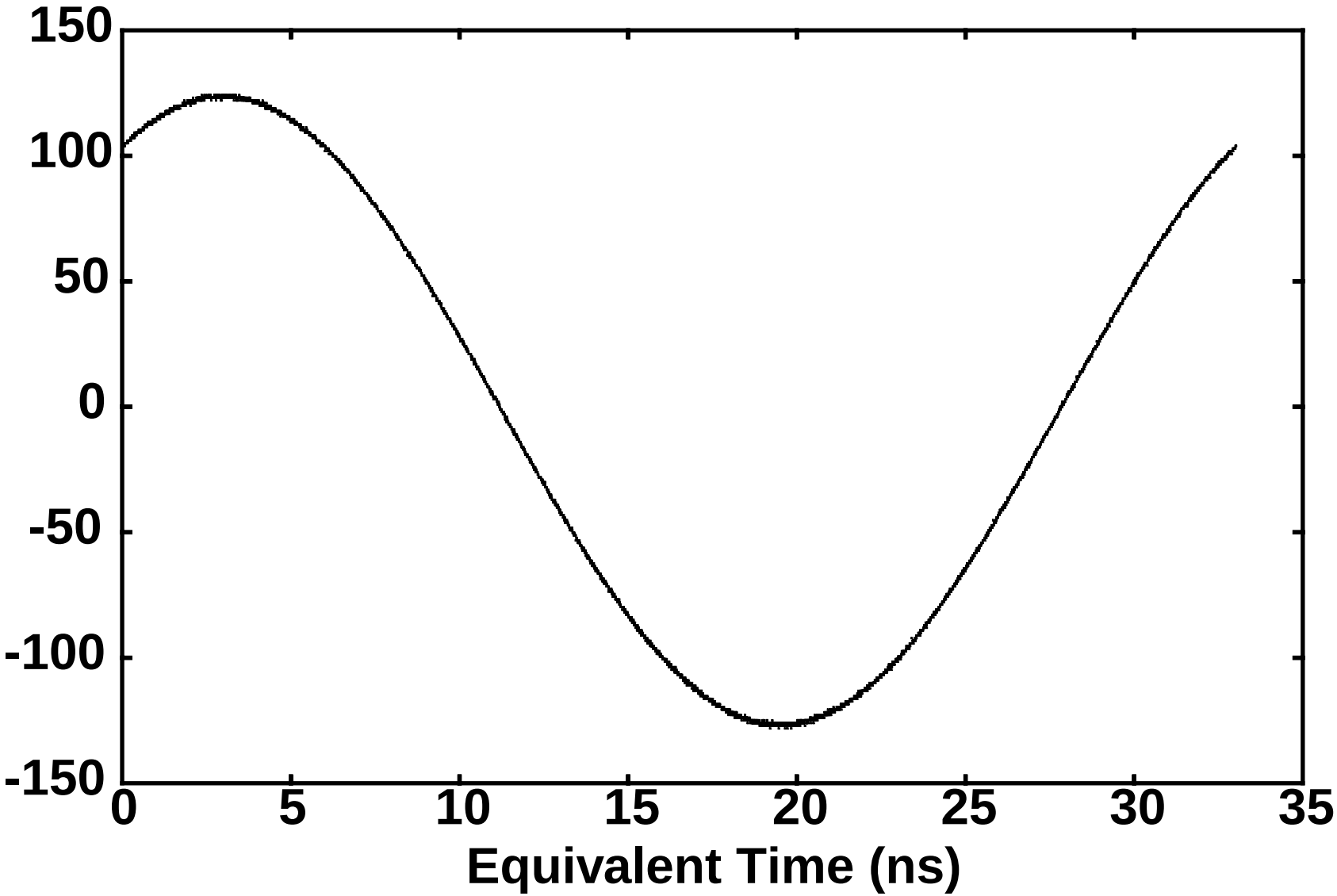

**7.1 mm x 4.0 mm** **300,000 FETs** **4.6 W** **0.35 μm**

# Acquisition Before Calibration



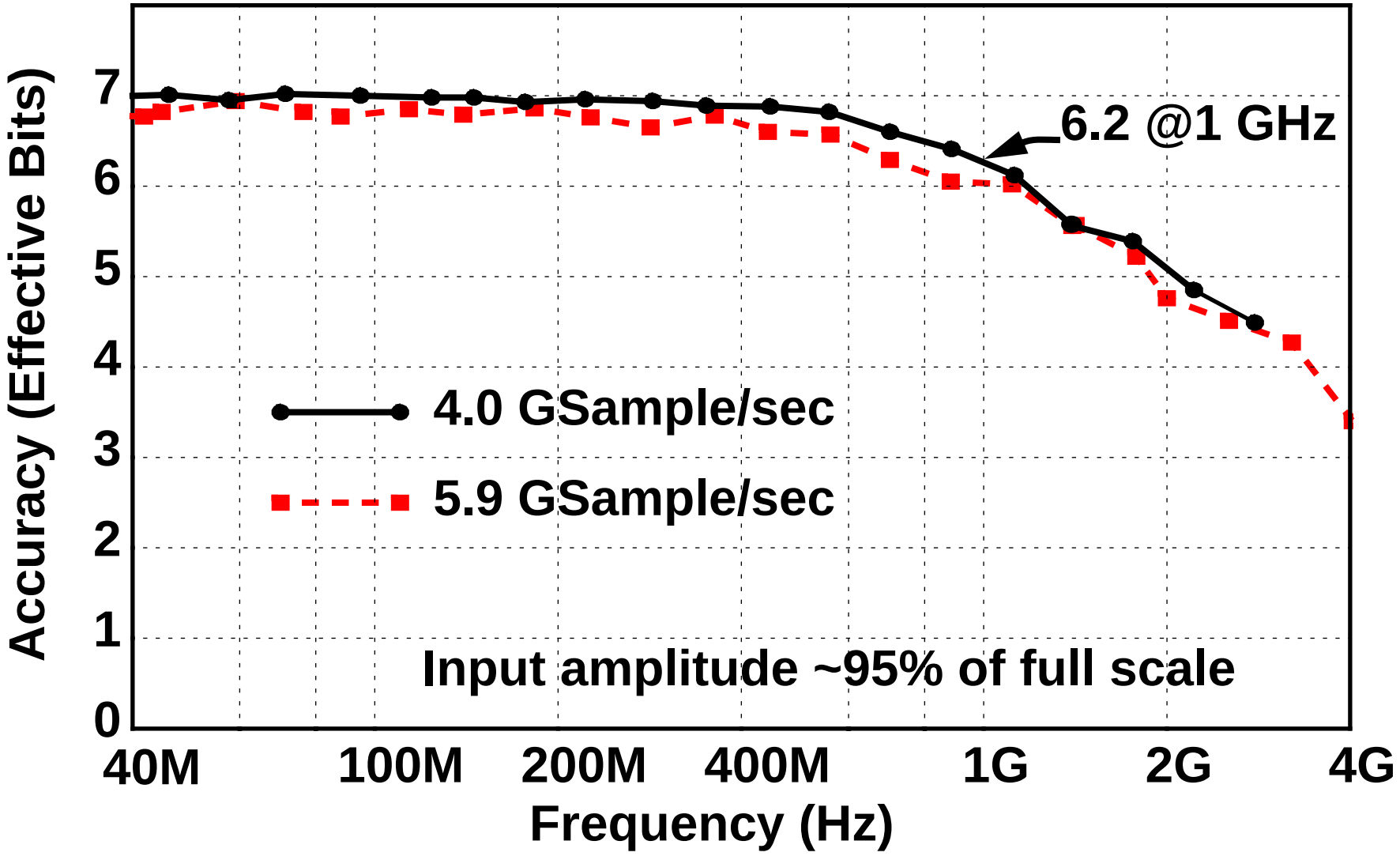

**~ 5 effective bits**

# Acquisition After Calibration



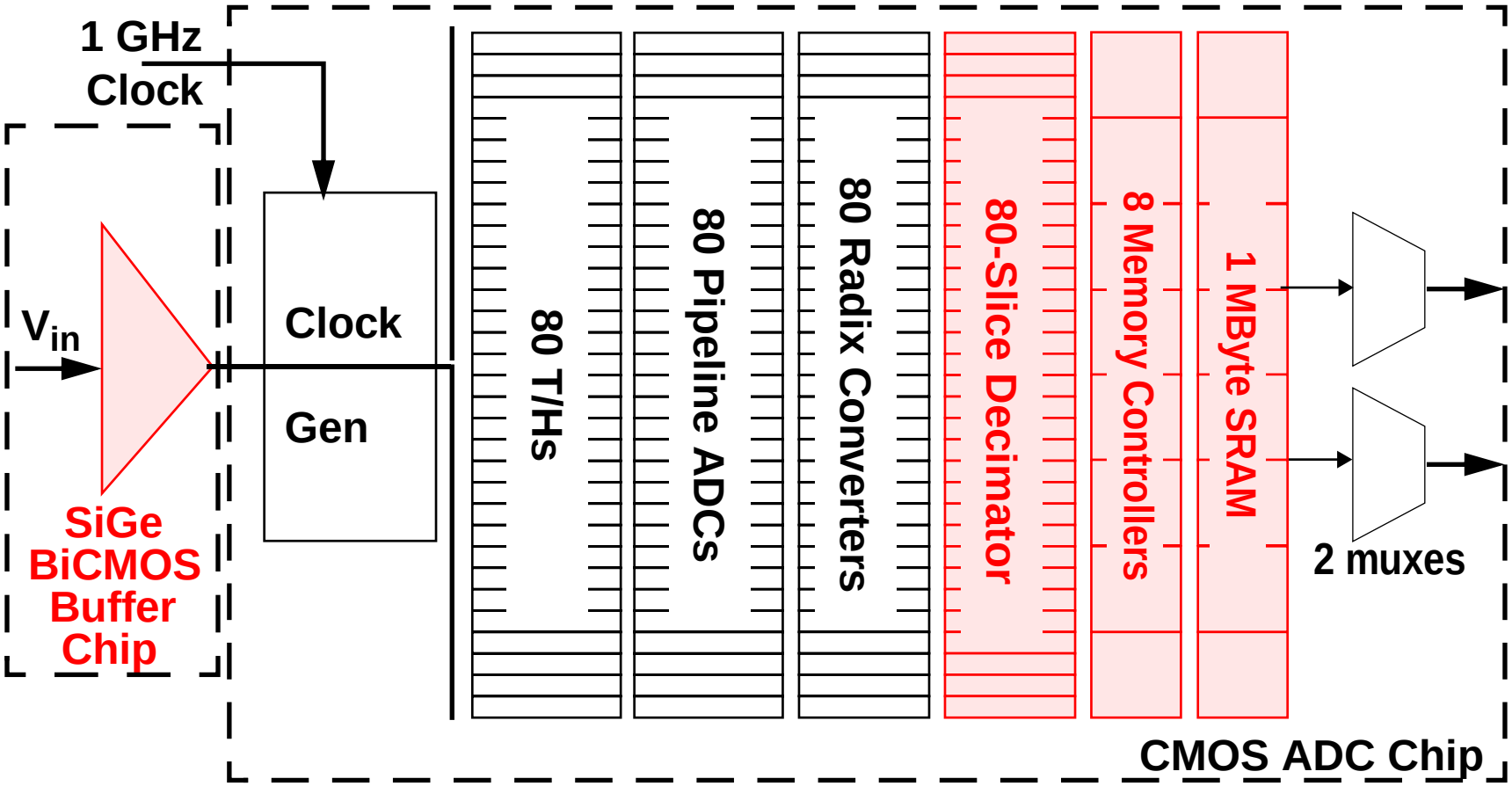

**$F_s$=4000 MSa/sec  $F_{in}$=30.27 MHz  7.0 effective bits**

# ADC Effective Bits vs Input Frequency



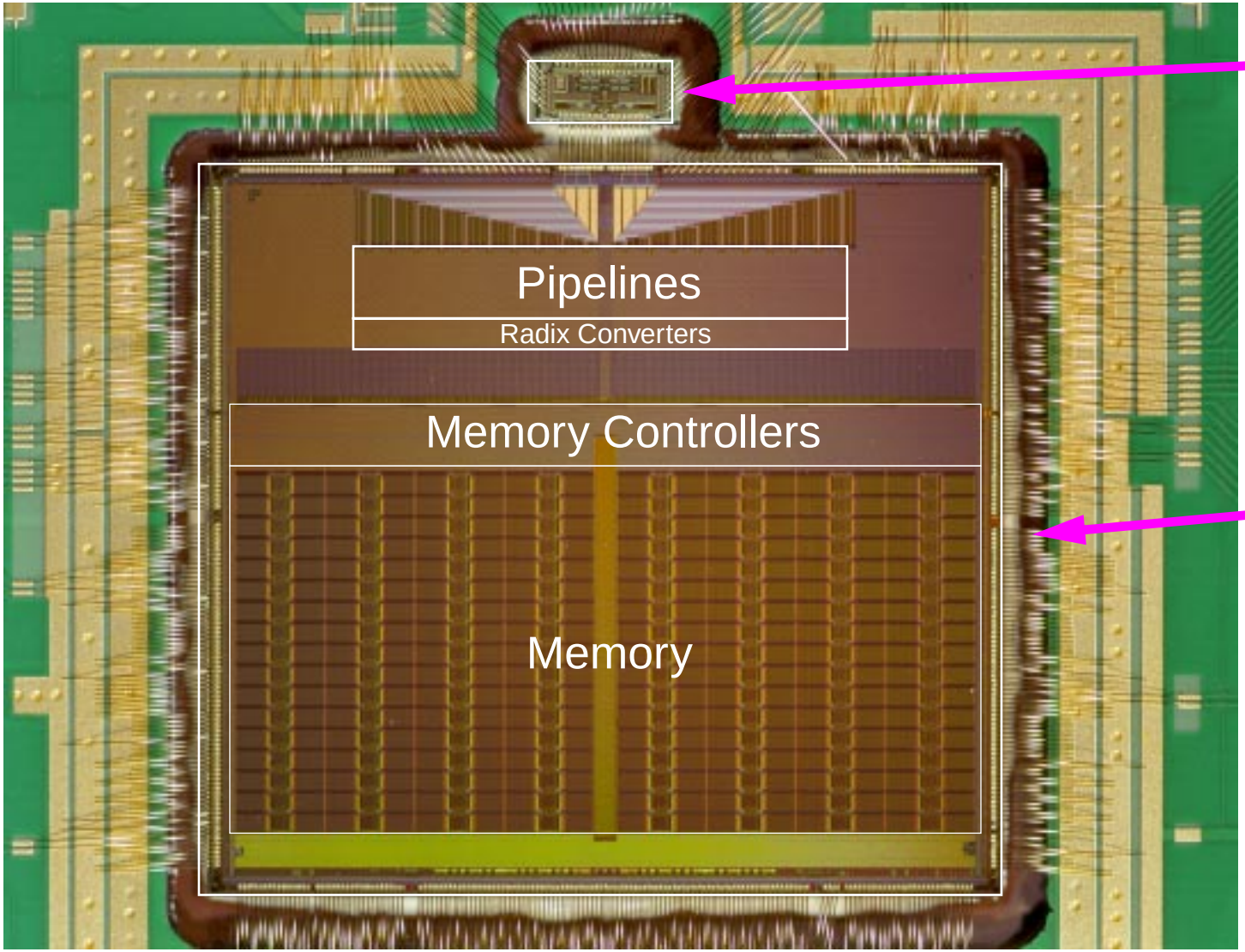

**1.2 ps rms clock error**

# 0.18 μm CMOS: 20 GSa/s, 6 GHz




- 2x faster process, 5x higher sample rate, 6x higher BW
- 80 ADC slices, larger $C_{in}$ --> SiGe input buffer chip
- 160 Gb/s data rate --> 1 MB on-board sample memory

# 20 GSa/sec ADC Module



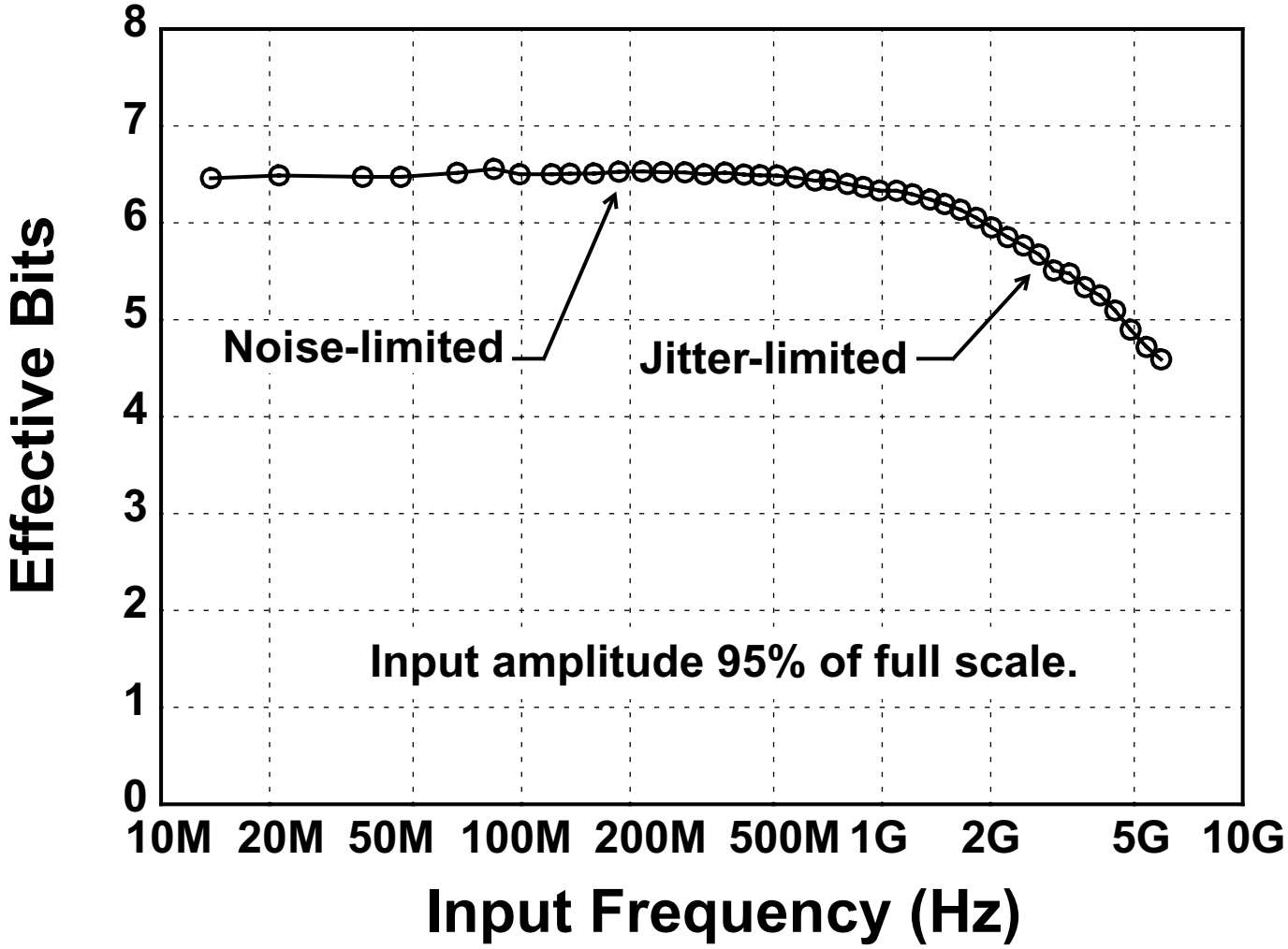

**Buffer:**
40 GHz SiGe
1 x 2 mm
1000 transistors
1 W

**ADC:**
0.18-um CMOS
14 x 14 mm
50M transistors
9 W

**Package:**
438-ball BGA
35 x 35 mm

➪ System Challenges: Low Voltage + Supply Droop
Digital Complexity

# ADC Effective Bits vs Input Frequency

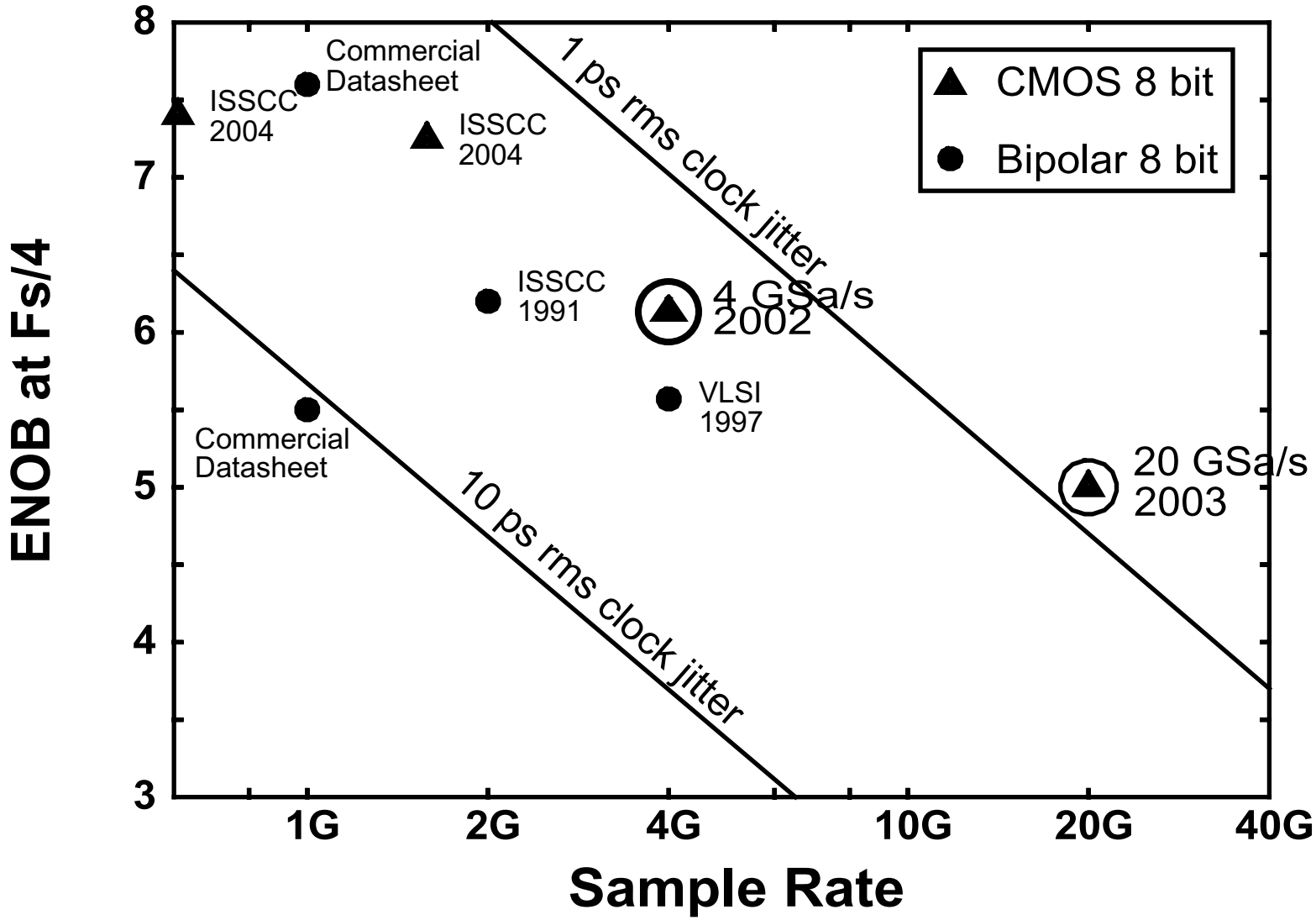



6.5 effbits at low frequency. 0.7 ps rms jitter

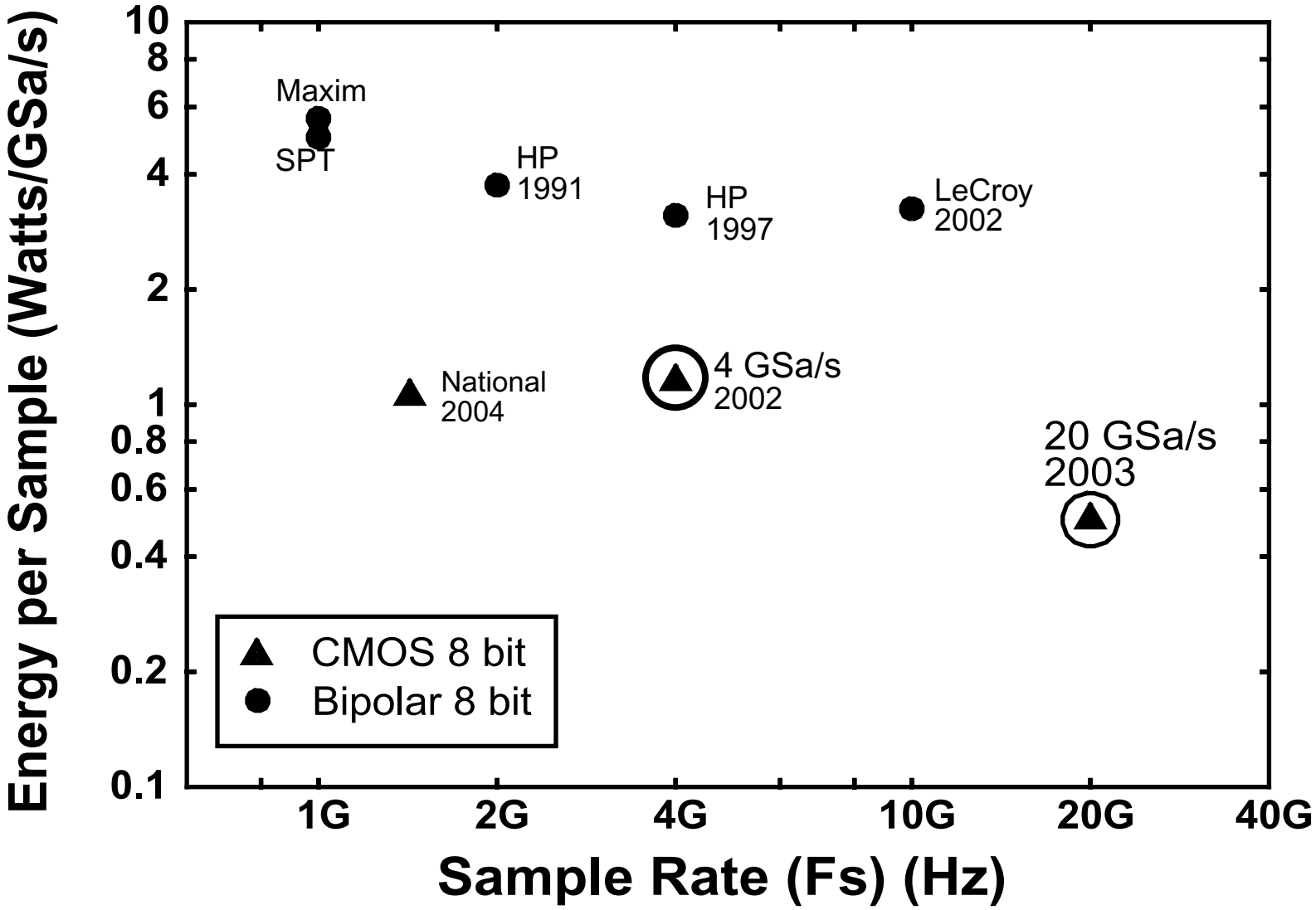
# ADC Chips - Key Specs

| | 4 GSa/s | 20 GSa/s | Units |
|---|---|---|---|
| Nominal Sample Rate | 4 | 20 | GSa/s |
| Resolution | 8 | 8 | bits |
| 3 dB Bandwidth | 1.6 | 6.6 | GHz |
| Accuracy @ 30 MHz<br>Fs/4 | 7.0<br>6.2 | 6.5<br>5.0 | effective bits (ENOB) |
| Timing Error (jitter) | 1.2 | 0.7 | ps rms |
| Noise | 0.6 | 0.9 | LSB rms |
| INL / DNL | ±0.3 / ±0.2 | ±0.4 / ±0.3 | LSB |
| Power | 4.6 | 10 | Watts |
| IC Technology | 0.35 μm | 0.18μm / 35GHz | CMOS / SiGe |
| Chip Size | 7.14 x 4.04 | 14x14 / 1x2 | $mm^2$ |
| Transistors | 300k | 50M / 1k | |
| Package | 27 mm | 35 mm | BGA |
| Memory | 0 | 1 M | samples |

# Monolithic ADCs in 2004



# Energy per Sample




- Twice the sample rate at 1/3 the power of the nearest competitor

# Conclusions

- Trends
  - Increasing importance of power efficiency and low cost
  - CMOS is taking over ever more of the ADC market
- Interleaved ADCs
  - Massive time-interleaving allows CMOS to compete at the highest sample rates
  - Very high BW possible with NMOS T/H
  - Calibration is a key to utilizing low-power, inaccurate circuits
  - The world’s fastest 8-bit ADC is now CMOS

# Acknowledgements

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