A 20 GSa/s 8b ADC with a 1 MB Memory in 0.18 μm CMOS

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Background

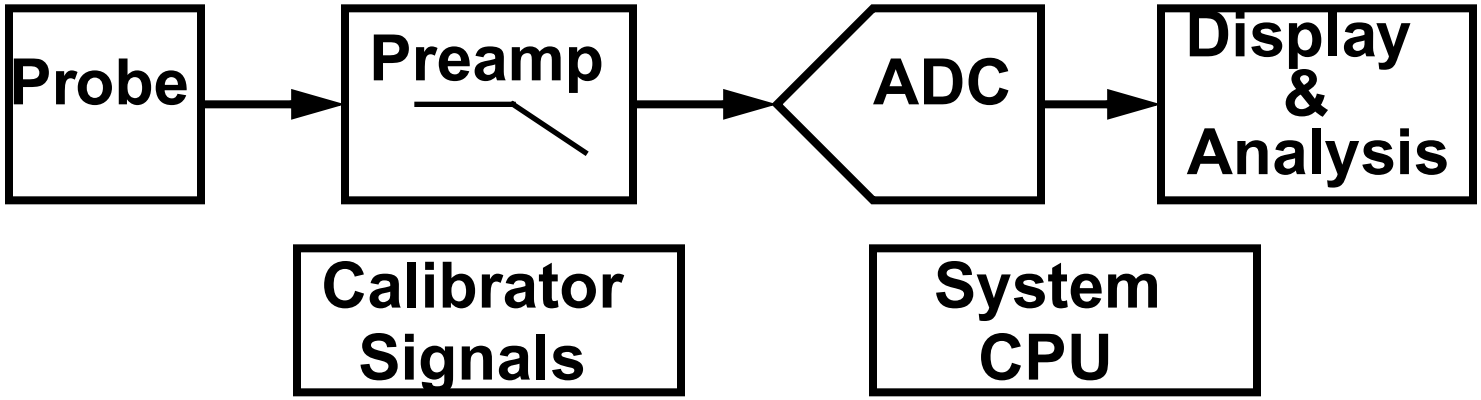
Design Goals:

- 20 GSa/s, 8-bit conversions
- -1 dB bandwidth of 6-GHz
- Low power (less than 15 Watts)
- On-chip memory for storage of 20-Gbyte/s data

Design Approach:

- Massively parallel interleaving
- Small transistors for low power
- Open-loop circuits for high speed
- Extensive calibration

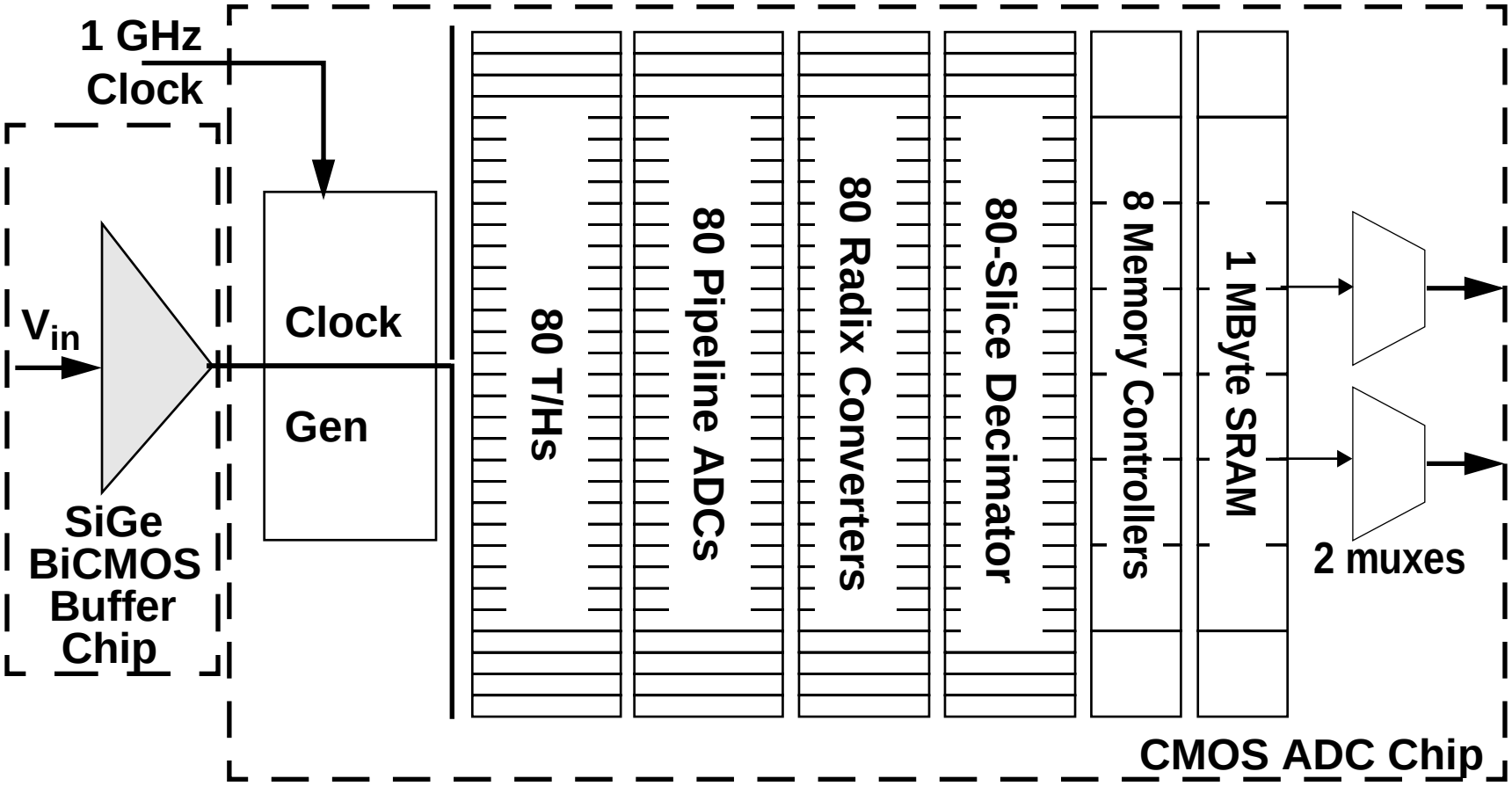
Application: Digital Oscilloscopes



Simplified oscilloscope block diagram

- Inputs band-limited to ~ Fsample/3.
- External calibrator signals. Calibration coefficients computed by system CPU.

ADC Module Block Diagram

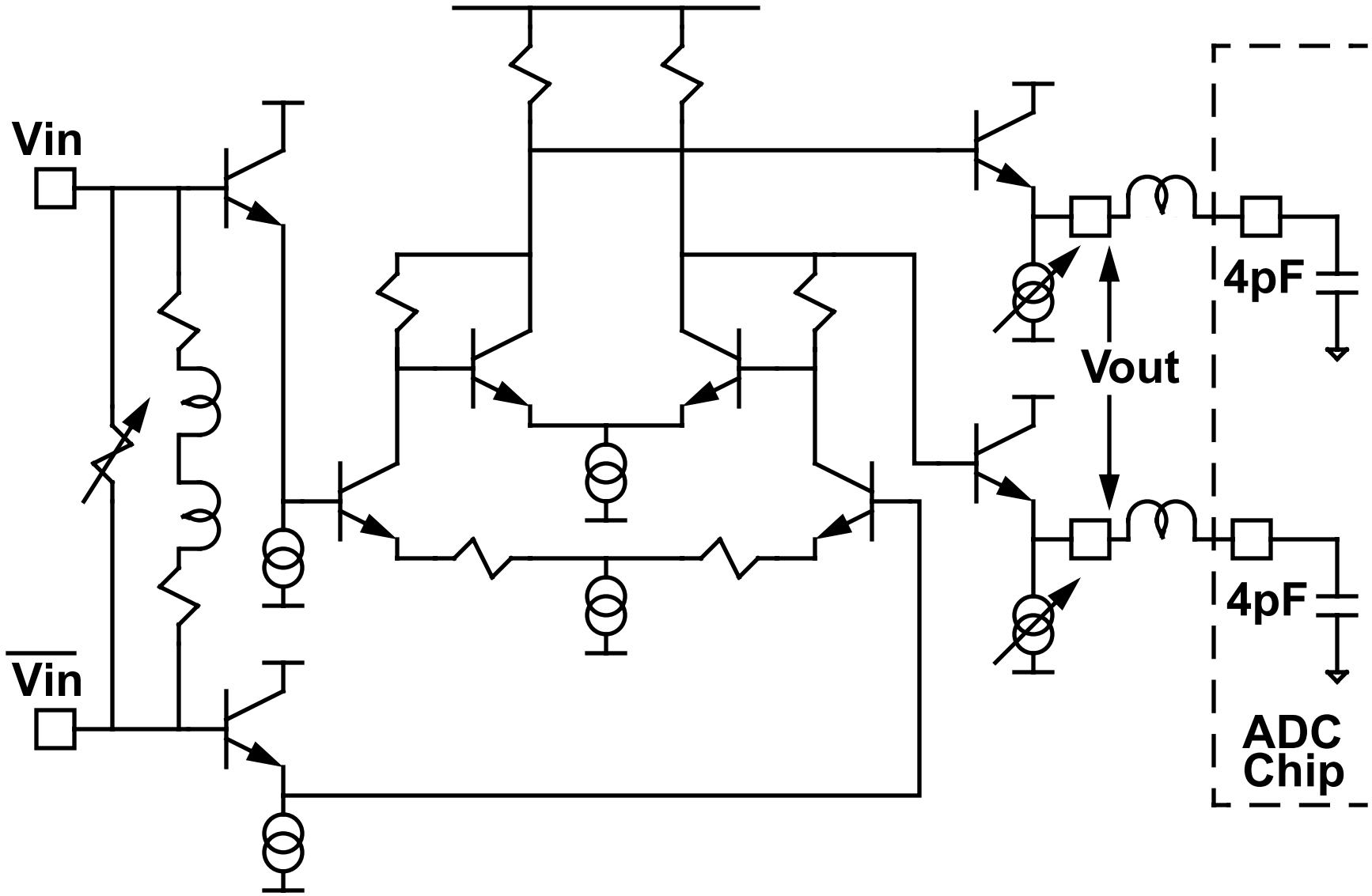


Input Buffer Chip

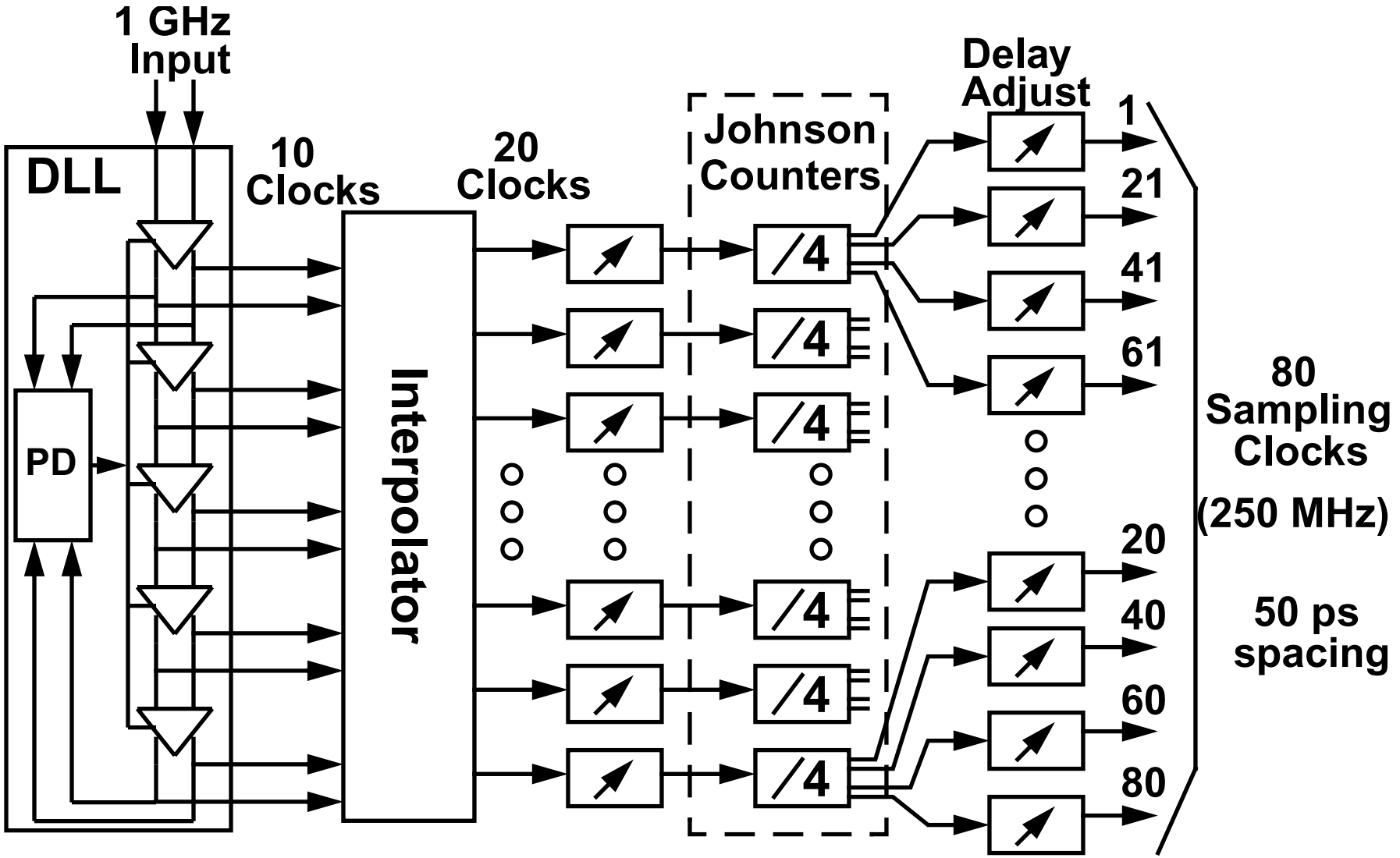
Design Goals:

- Flat gain response from DC to 6 GHz.
- Drive the ADC chip's 4pF input capacitance through chip-to-chip wirebonds.
- Well-matched 50-ohm input termination.
  - Low input capacitance.
  - Adjustable input resistance.

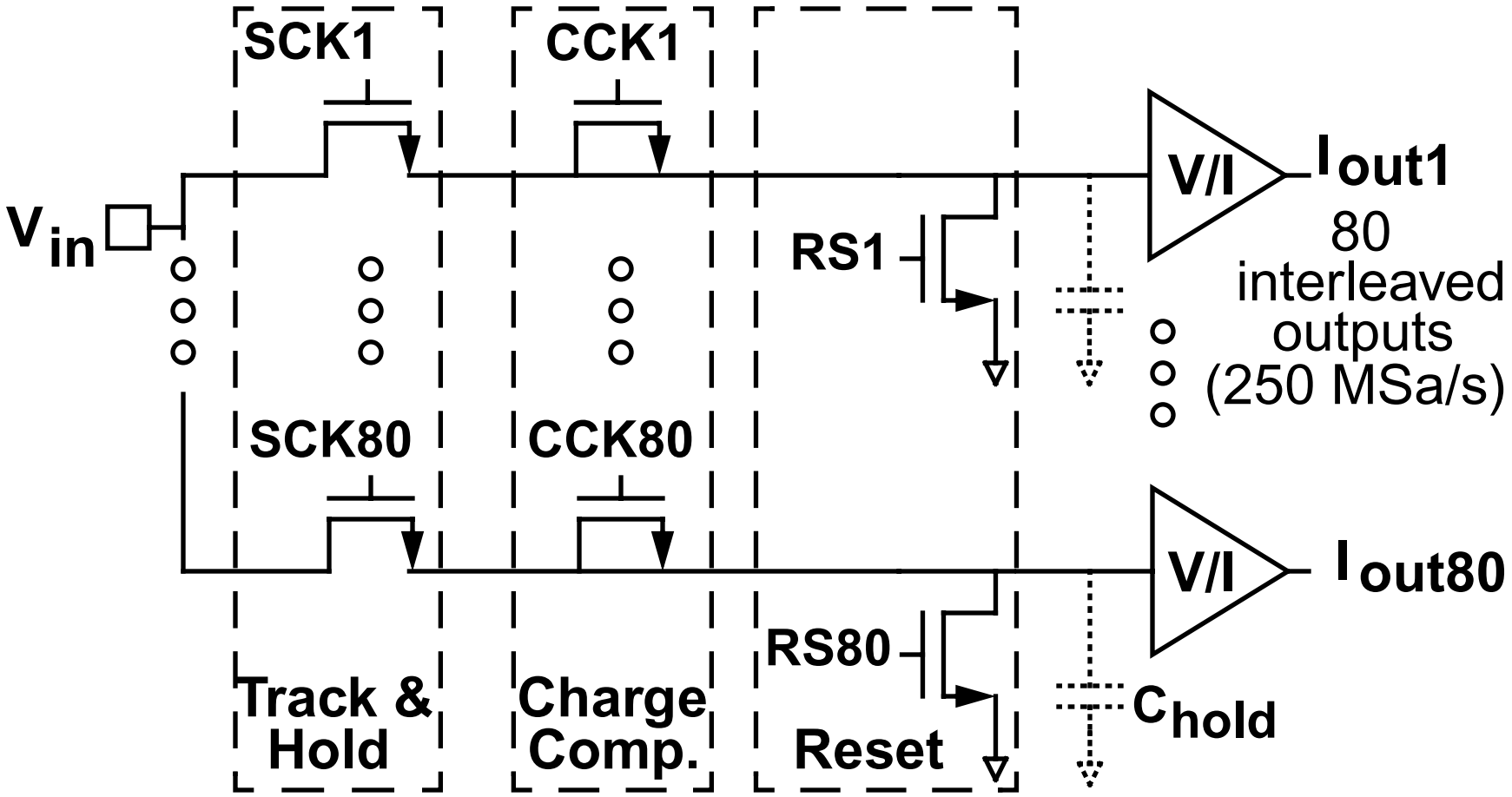
Simplified SiGe buffer chip schematic



Clock Generator



Track and Hold Front End



- Full 6-GHz signal bandwidth at C_{hold}.
- Transconductor (V/I) output drives pipeline ADC.
- Reset prevents signal-dependent kickback onto V_{in}.

Pipeline ADC

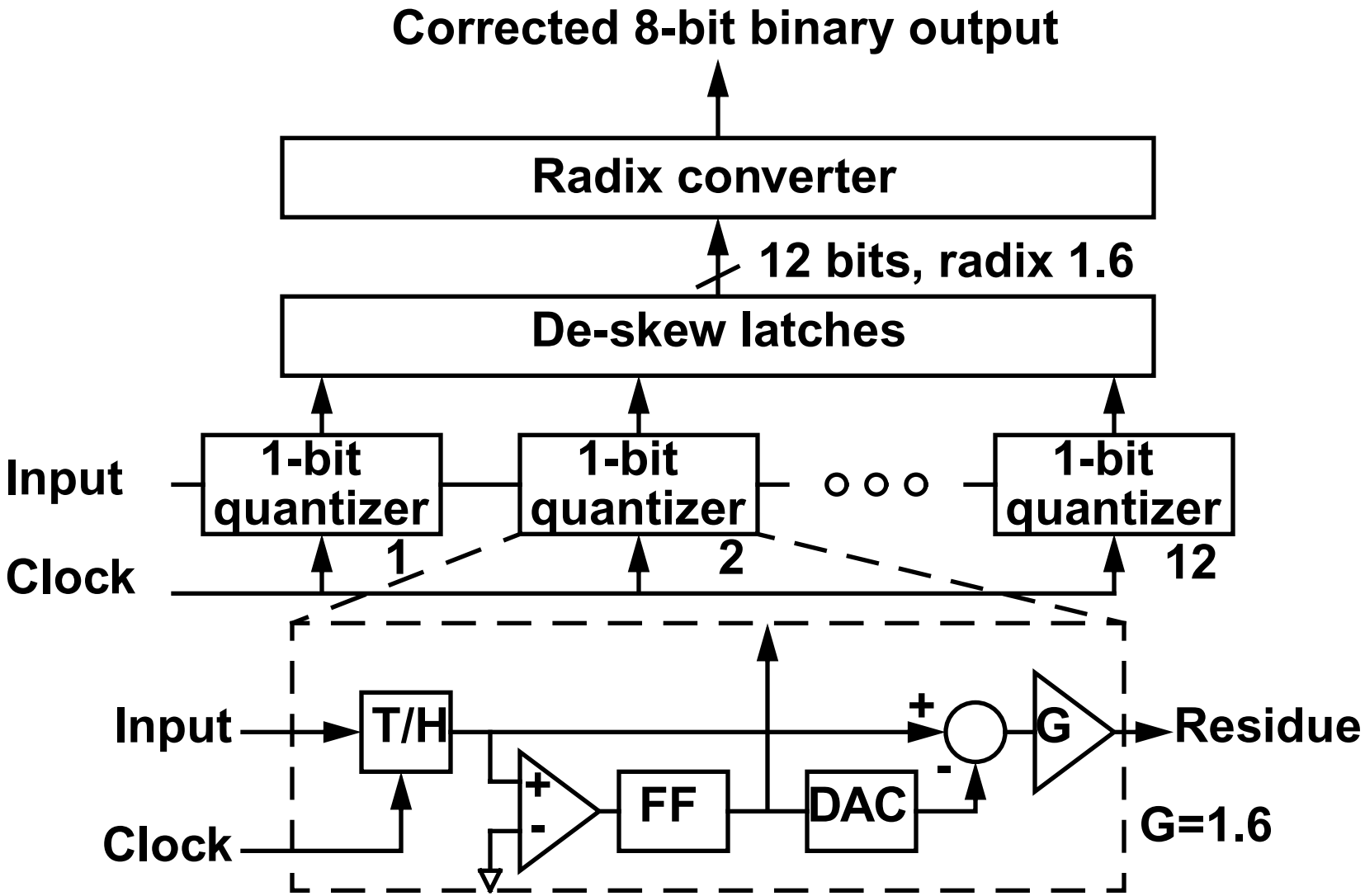
Required performance:

- 250 MSa/s.
- 8 bits.

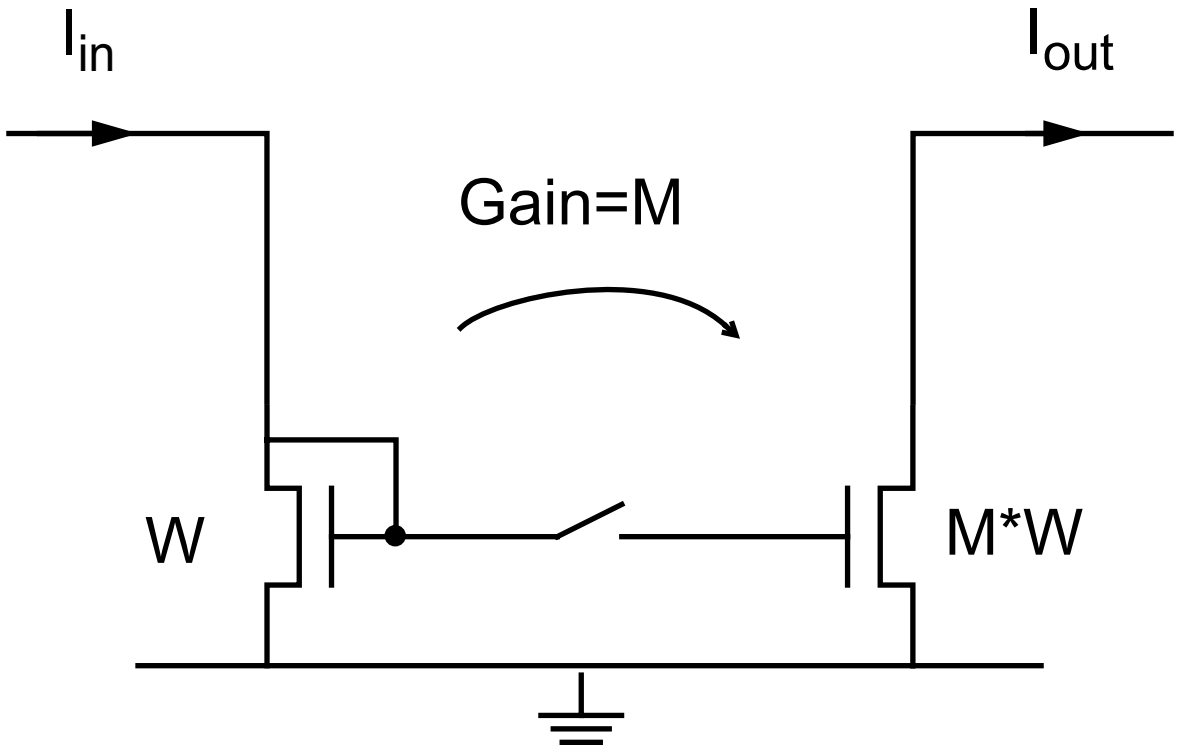
Design approach:

- One bit per stage pipeline ADC for high speed.
- Open loop amplifiers for fast settling.
- Reduced radix for redundancy.
- Current-mode signals enable simple amplifiers that occupy minimal area.

Pipeline ADC Block Diagram

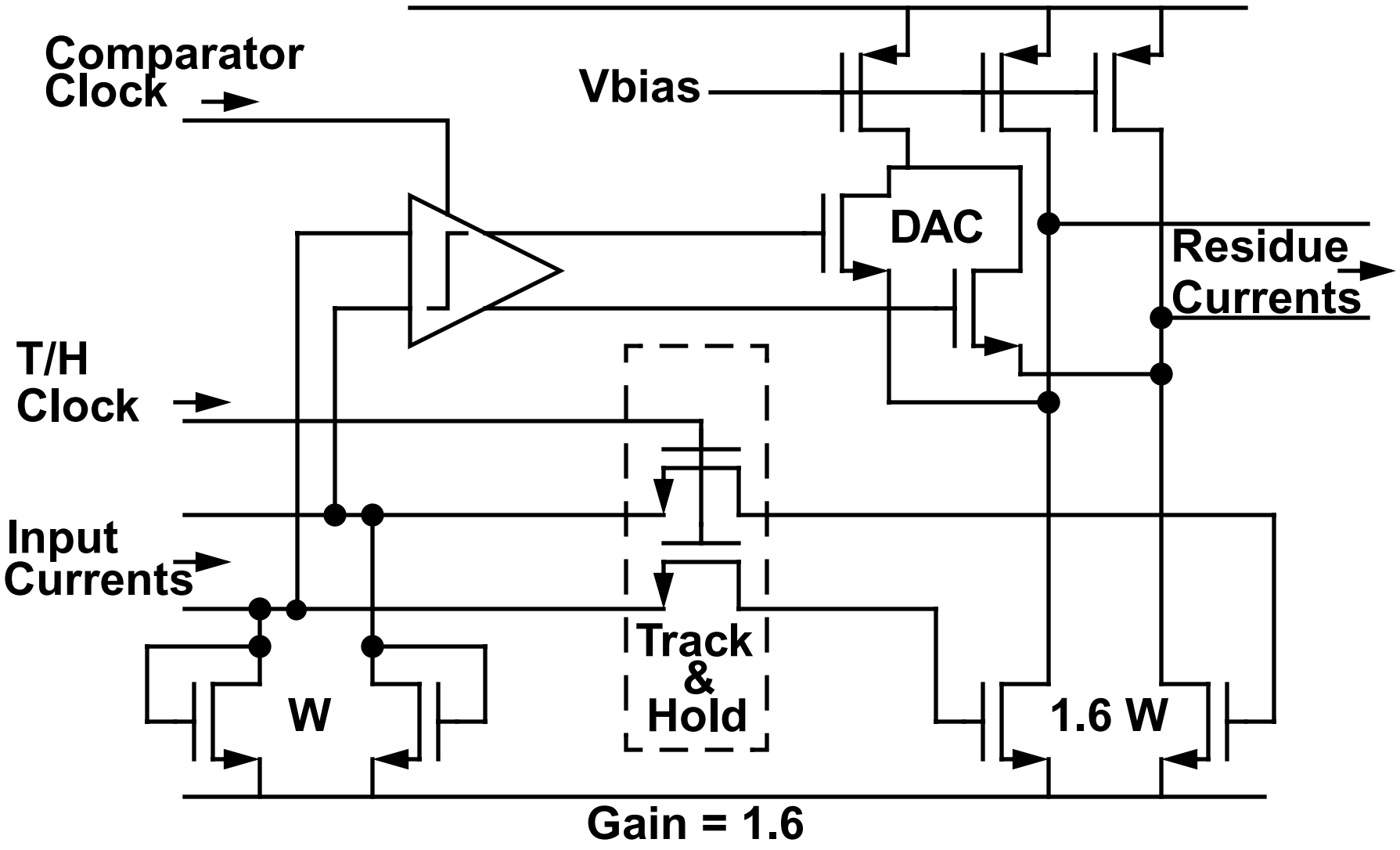


Current-Mode T/H and Gain



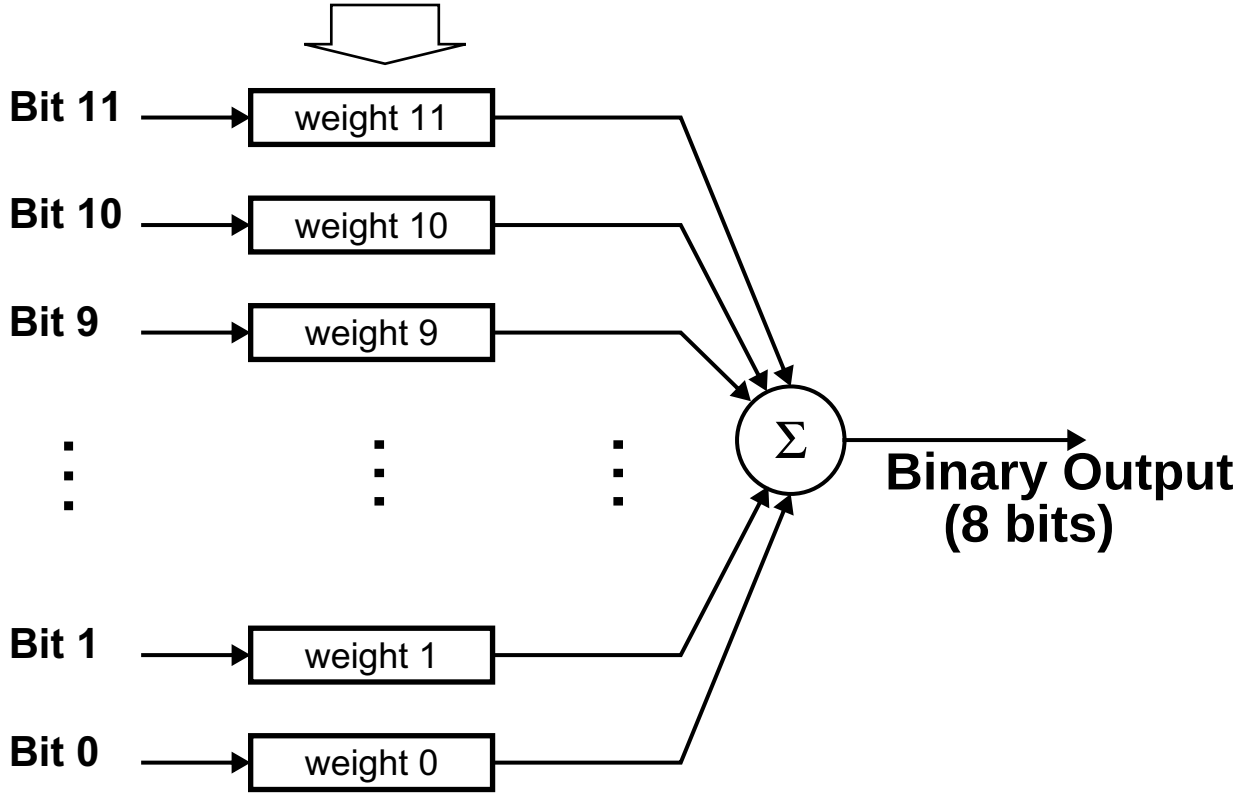
- Good Linearity: Current mirrors with cascodes are 8 bit linear.
- Poor Accuracy: Gain and offset errors.

Simplified Pipeline Stage Schematic



Radix Converter - Principle of Operation

Calculate and download bit weights during calibration.



$$\text{Output} = b_{11}.w_{11} + b_{10}.w_{10} + \ \ldots \ + b_1.w_1 + b_0.w_0$$

- Look-up table would be an alternative architecture.
- This ADC uses a hybrid look-up/adder.

Pipeline ADC Performance

Outstanding speed/power ratio

- 250 MSa/s
- 57 mW total
  - 9 mW V/I buffer
  - 28 mW pipeline
  - 20 mW radix converter

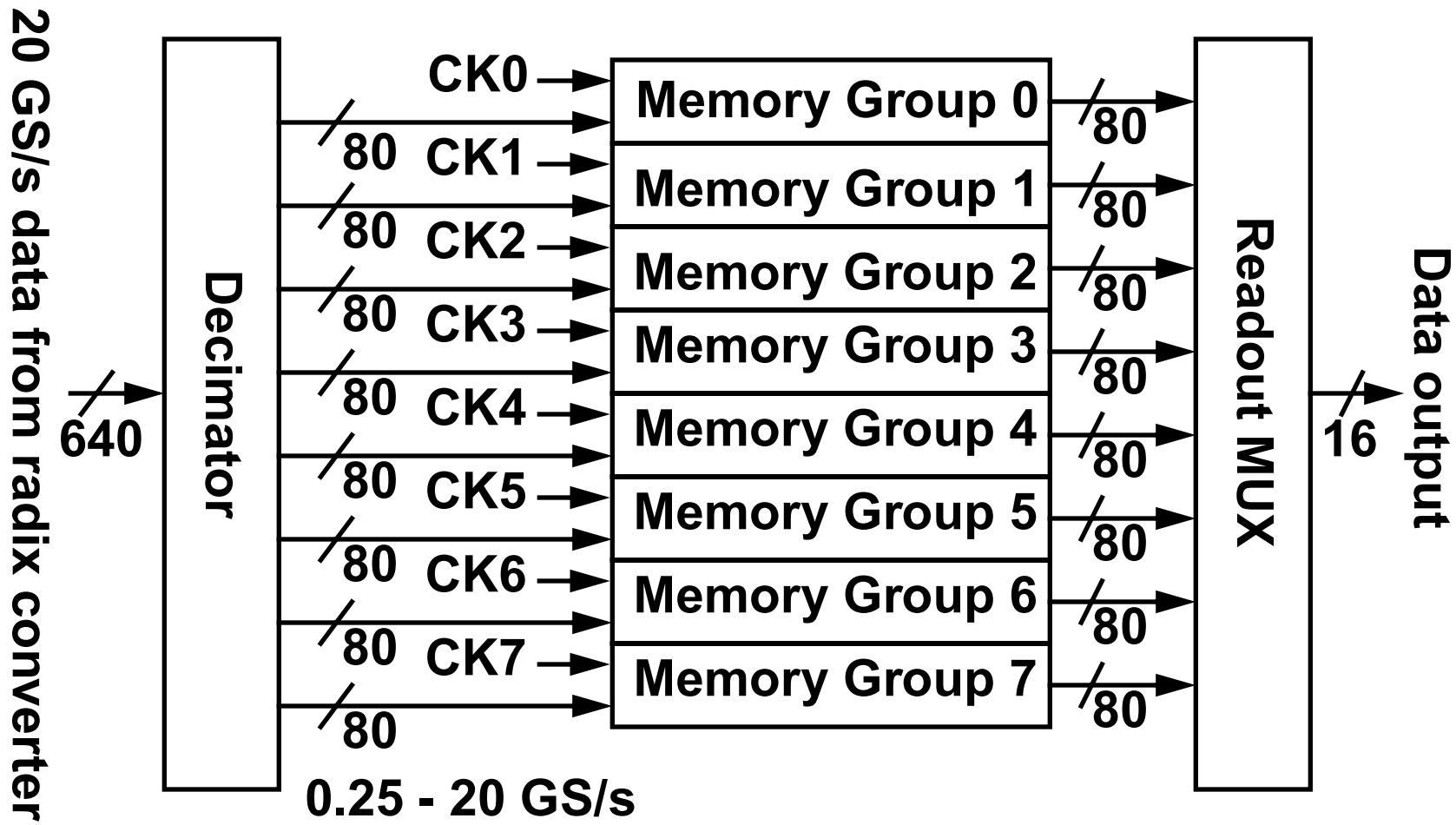
Small area

- 0.12 mm^2

On-chip Memory System Goals

- Full-speed 160-Gbit/sec data storage.
- Store data at user-selectable sample rates.
- 1-Mbyte storage capacity.
- Low digital noise coupling to analog circuits.
- Low impact on fabrication yield.
- Memory controller synthesized from Verilog.

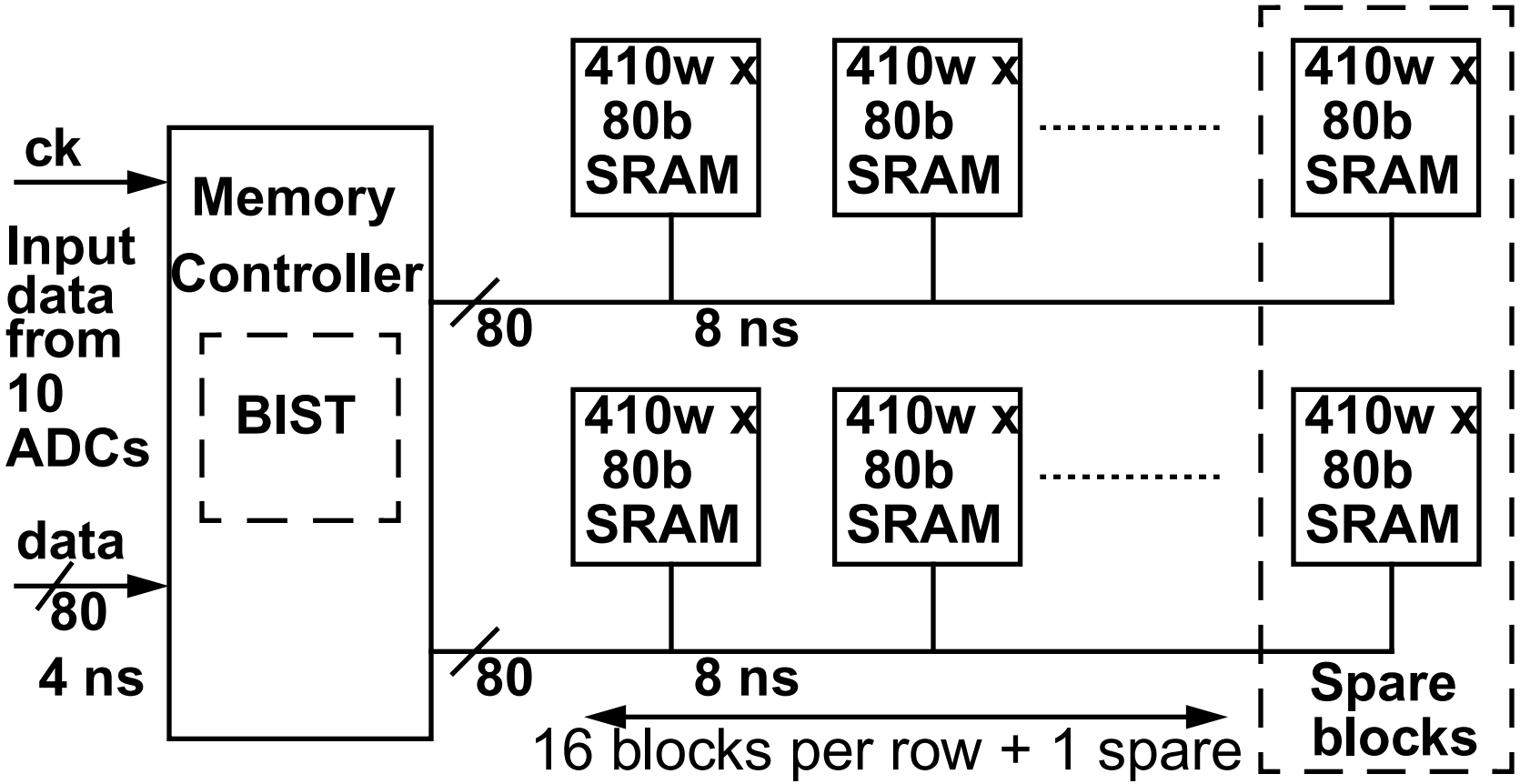
Memory System Block Diagram



Memory Design Approach:

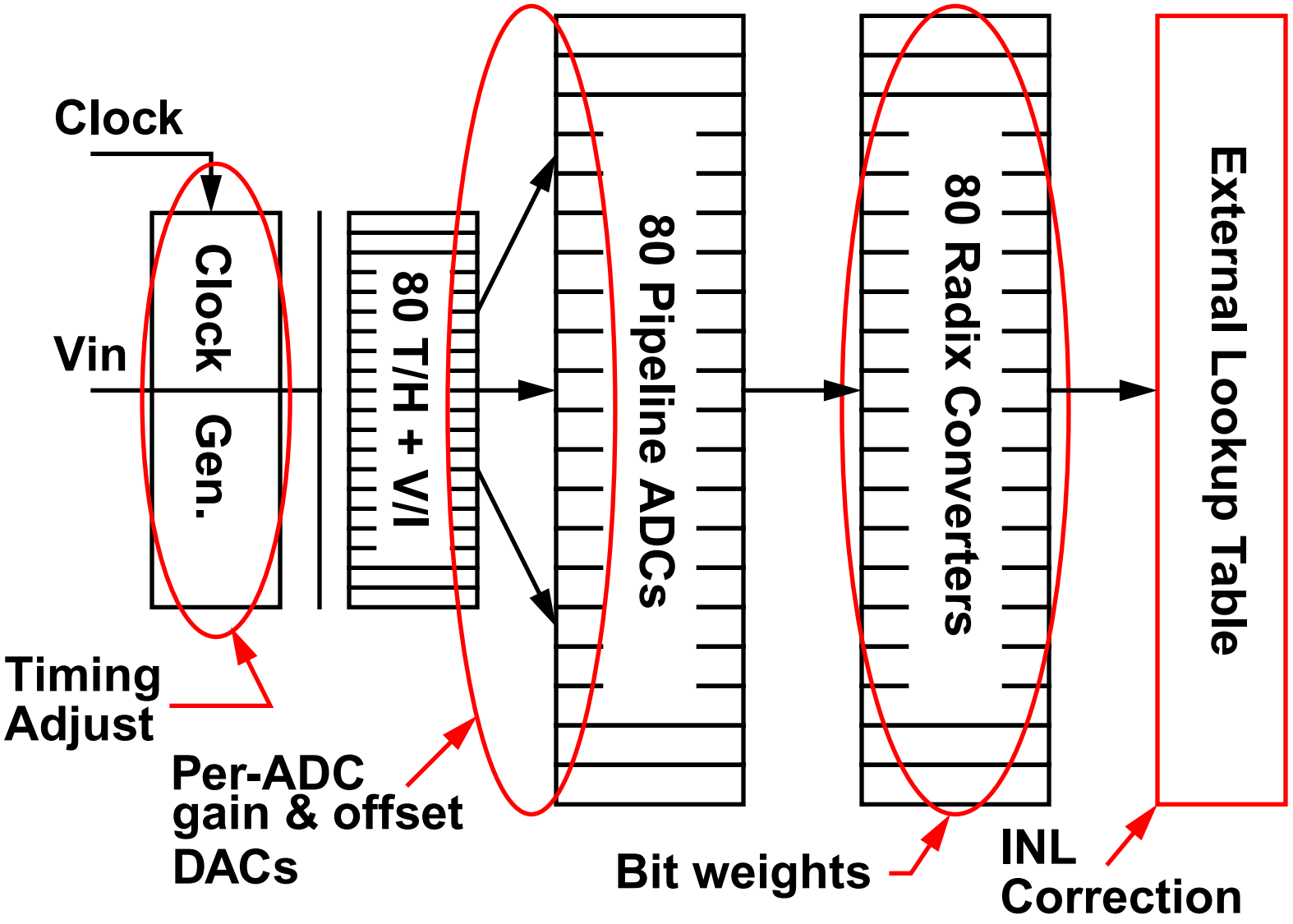
- Programmable decimator for adjustable sample-rate storage.
- Static RAM with built-in self test (BIST) and redundancy.
- Staggered writes
  - Full-width data path is 80 * 8 bits = 640 pairs.
  - 8 memory group clocks staggered at 0.5-ns intervals to spread out supply-current spikes.
- Dummy writes during non-acquisition intervals keep chip temperature constant and maintain calibration accuracy.

Memory Group (1 of 8)



- BIST runs at power-up.
- Defective blocks are auto-detected and replaced by spares.
- Precharged data lines minimize pattern-dependent noise.

Calibration



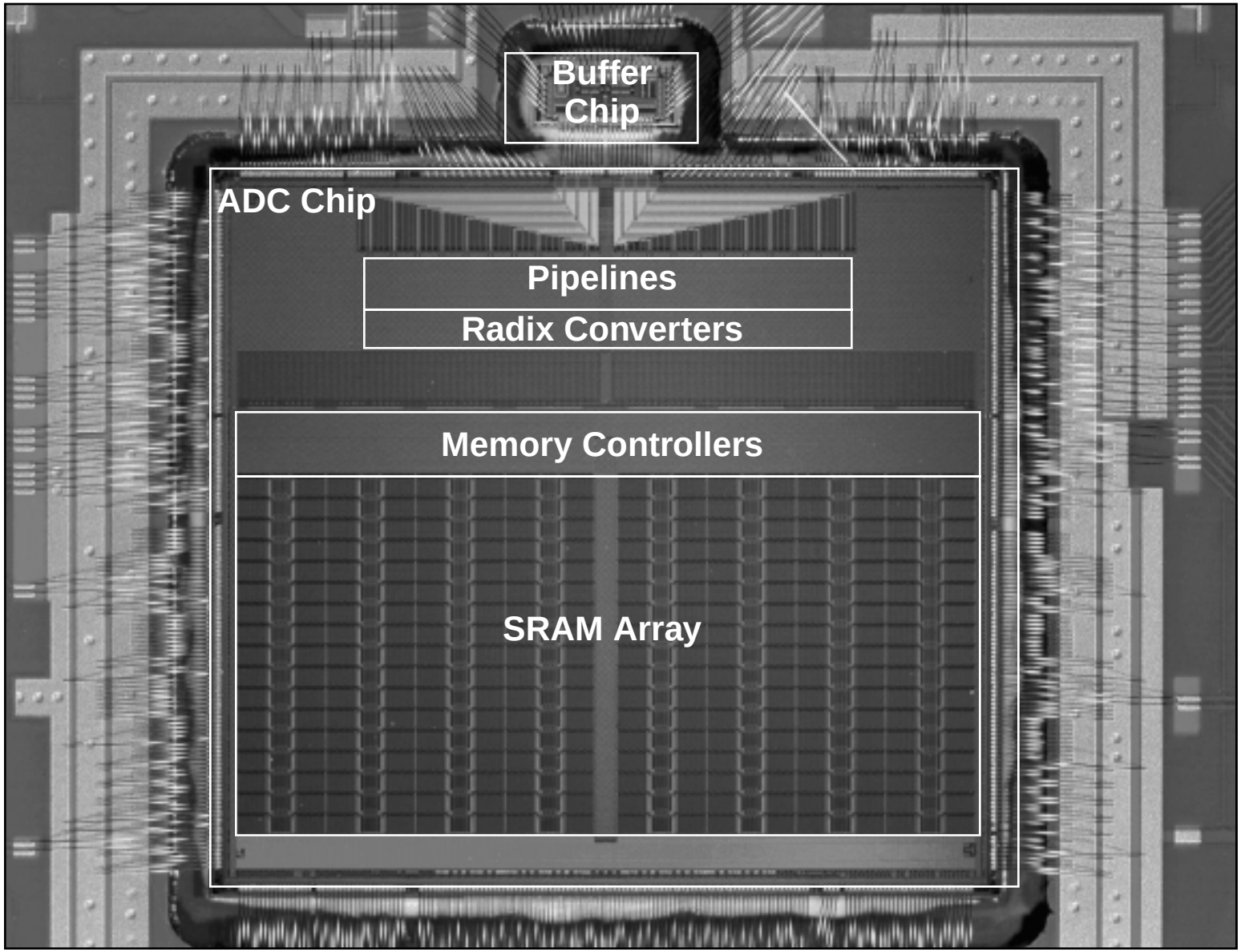
Offline Calibration

Voltage Calibration

- Apply a slow ramp input, observe ADC radix bits.
- Adjust analog gain and offset for each path.
- Use least squares fit on a large record to find optimal bit weights and 3rd harmonic fit.
- Least squares fit minimizes INL.

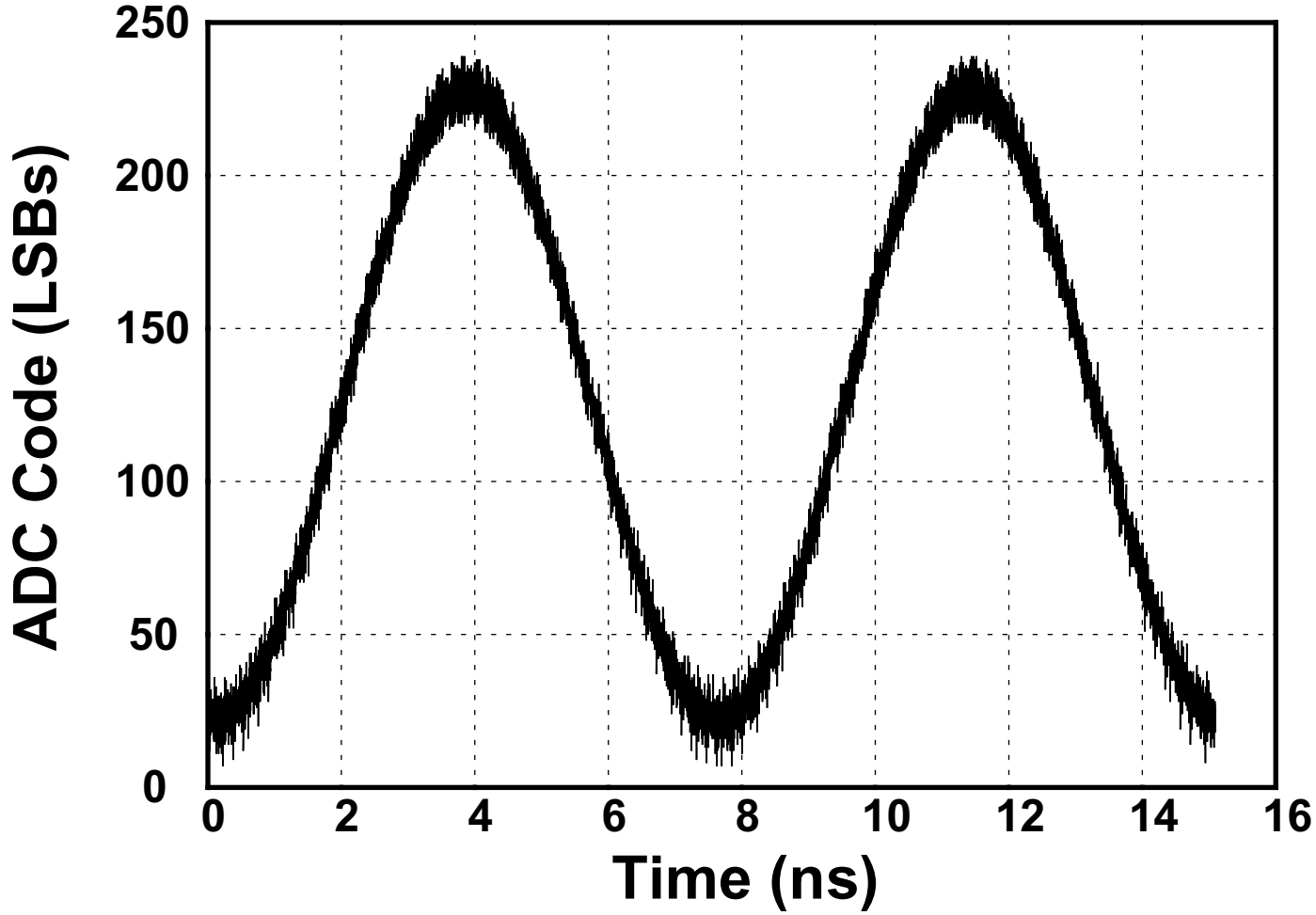
Timing Calibration

- Apply a pulse train with fast edges.
- Use an FFT to measure phase delay on each T/H.
- Adjust time delays and iterate.



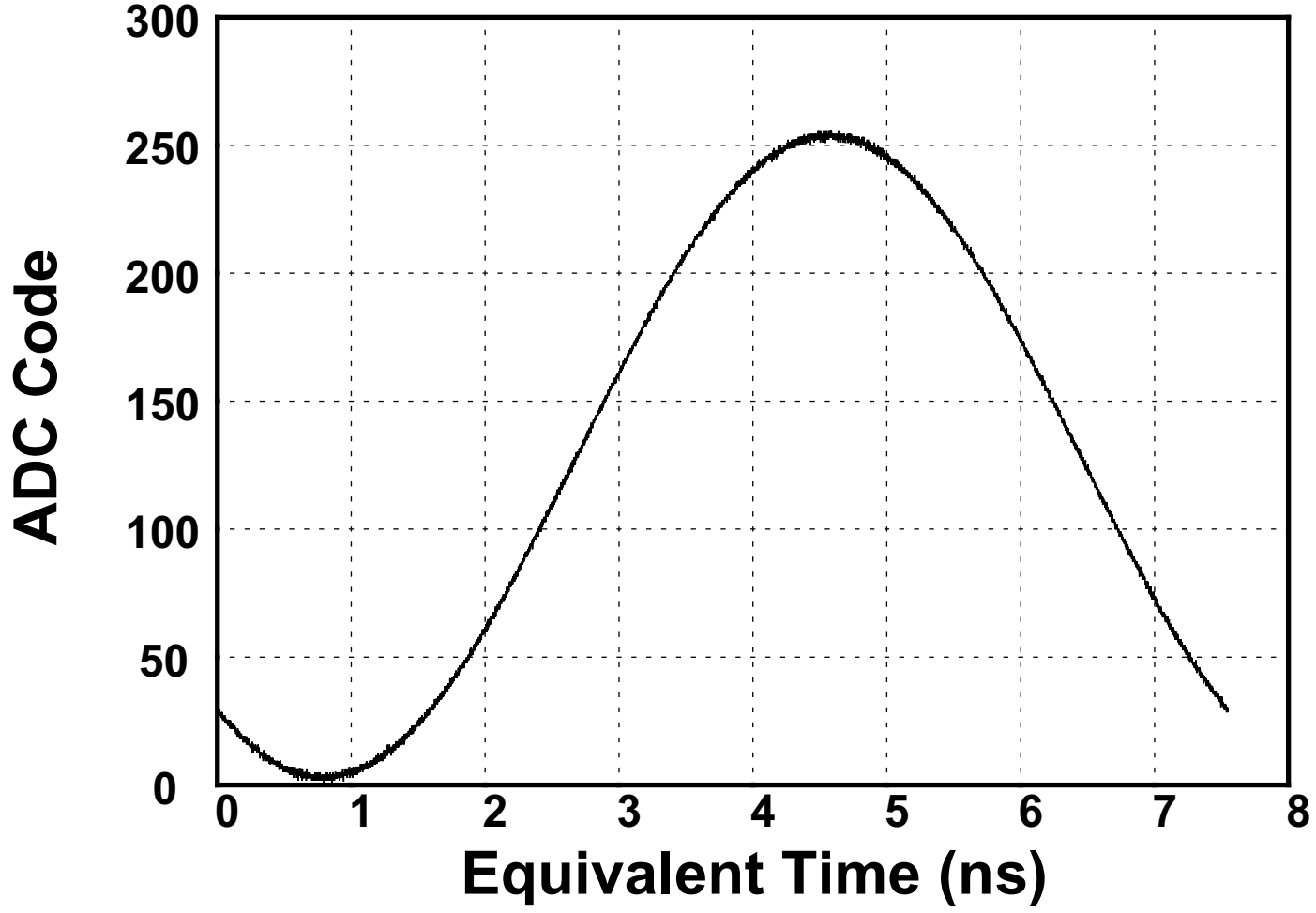
1.2 x 2.6mm buffer chip, 14 x 14mm ADC chip.

Acquisition Before Calibration



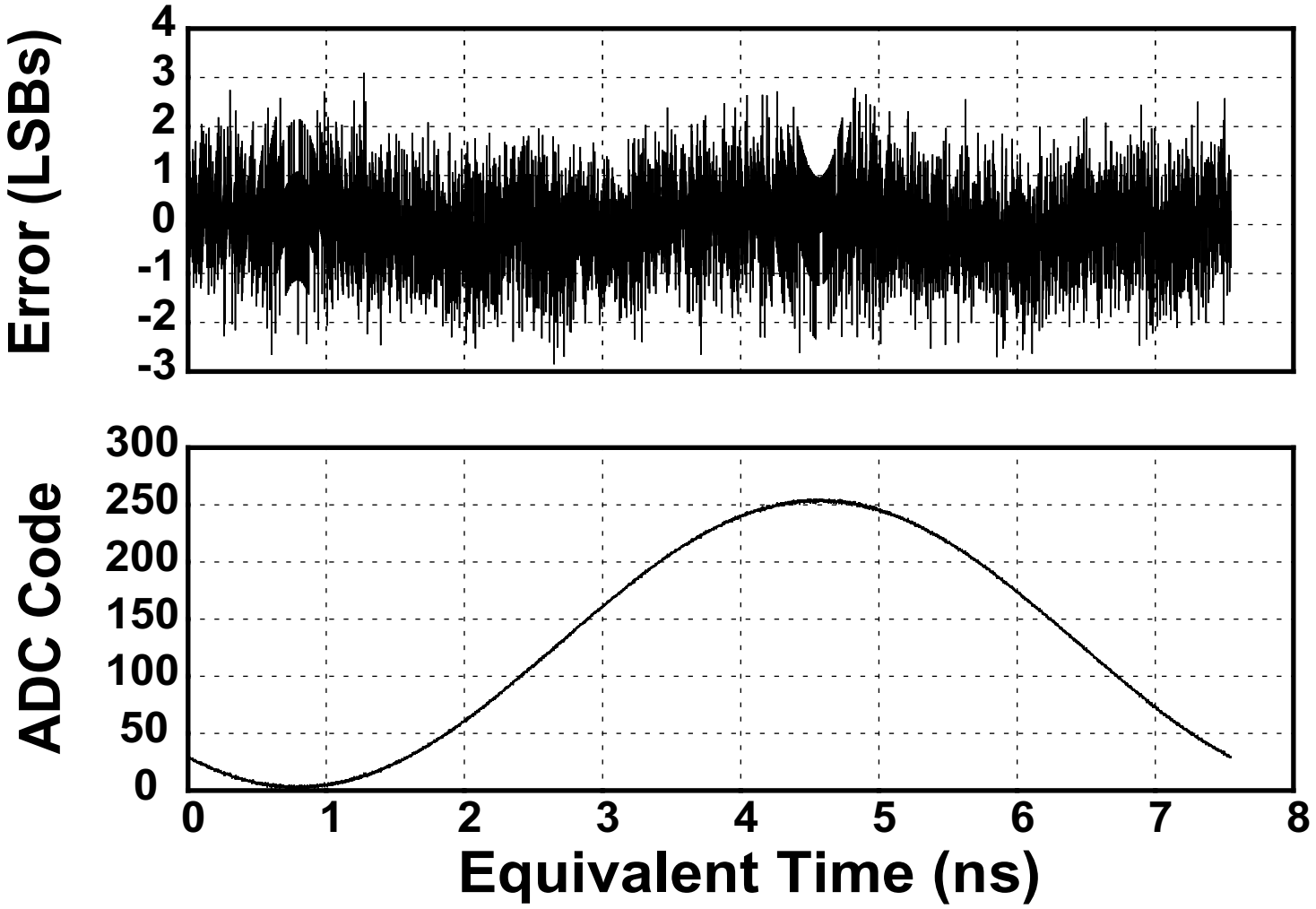
~ 3.5 effective bits

Acquisition With Calibration



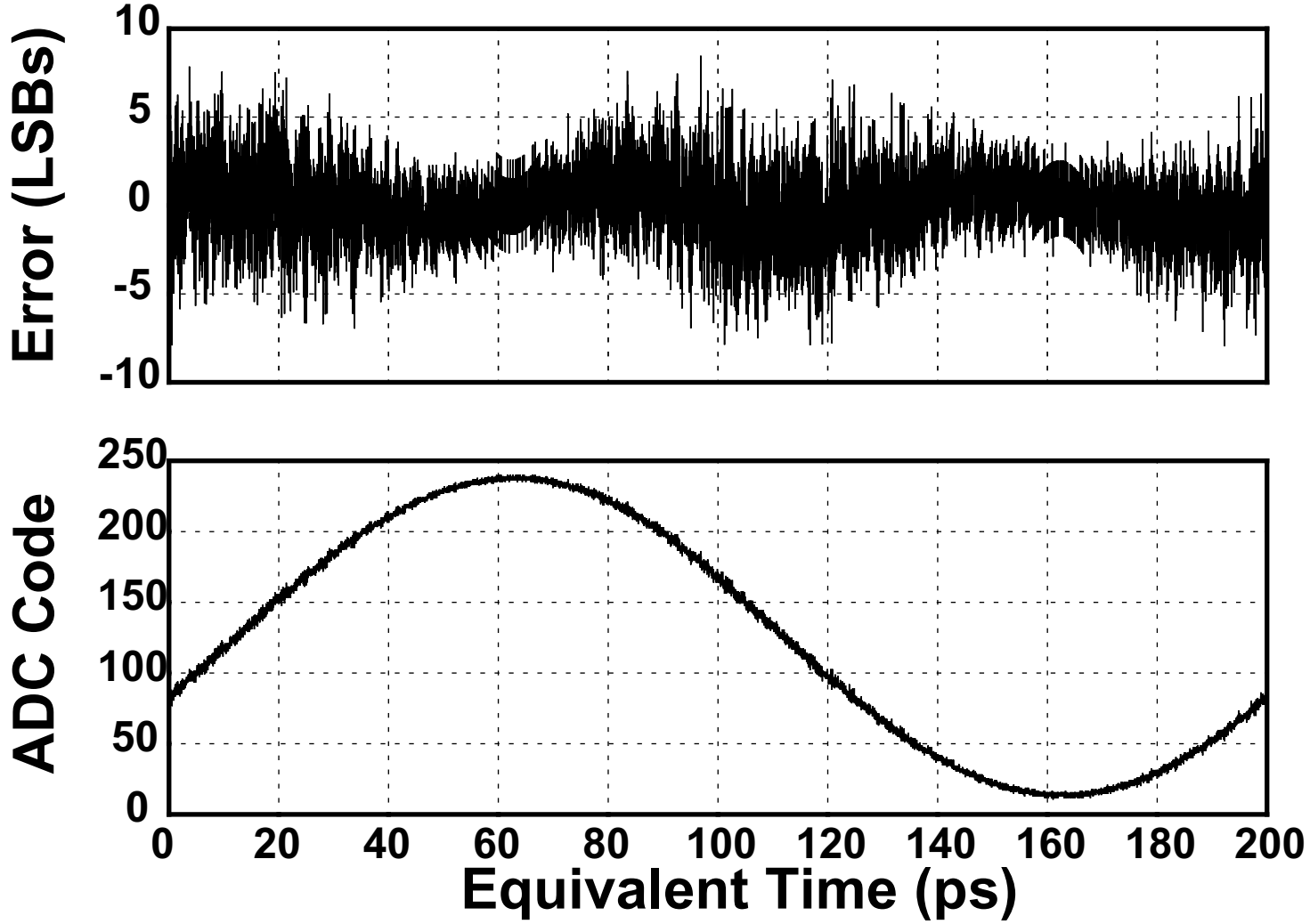
Fs = 20 GSa/s Fin = 132.5 MHz 6.4 effective bits

Acquisition With Calibration



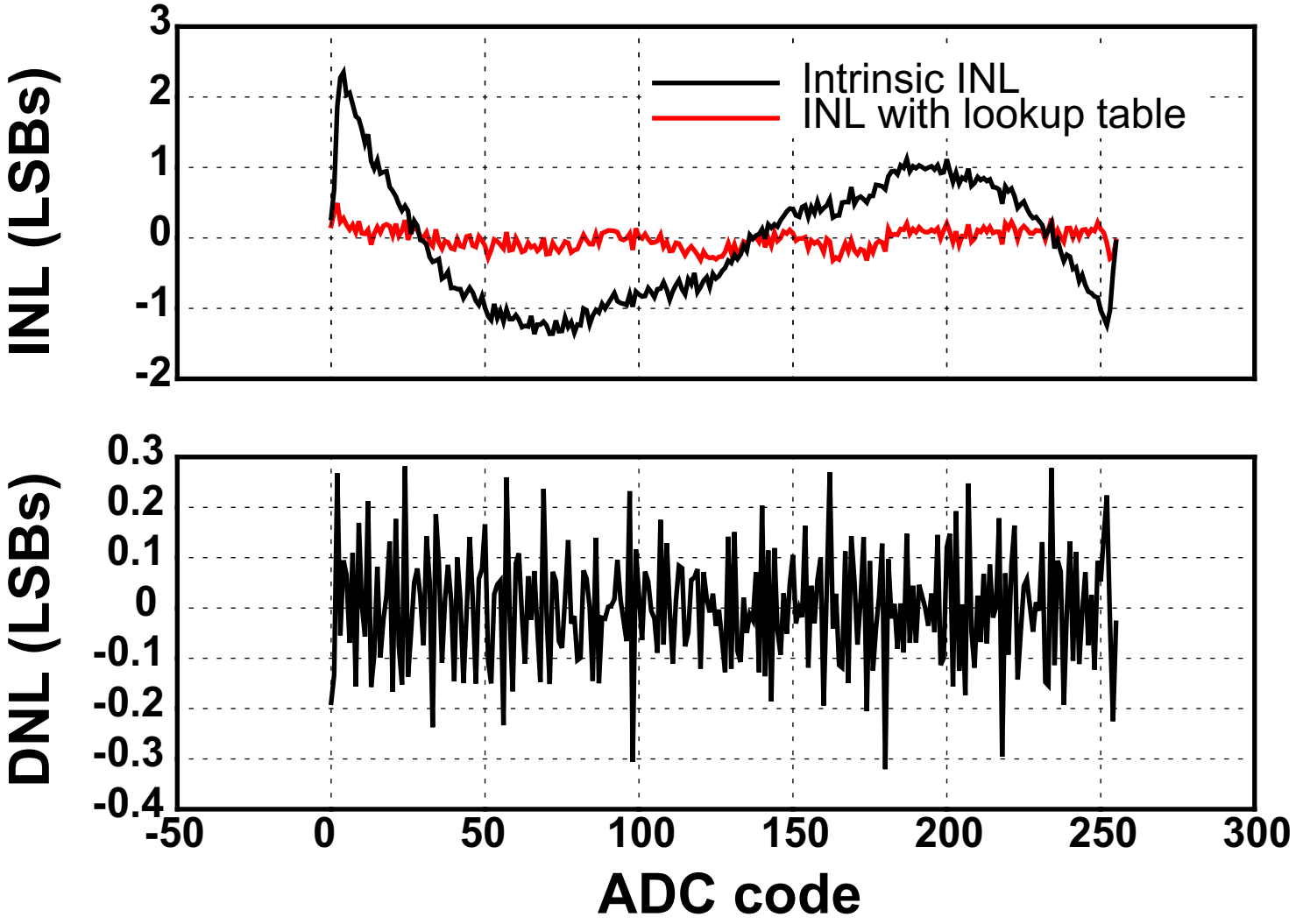
Fs = 20 GSa/s Fin = 132.5 MHz 6.4 effective bits

Calibrated, With 5 GHz Input

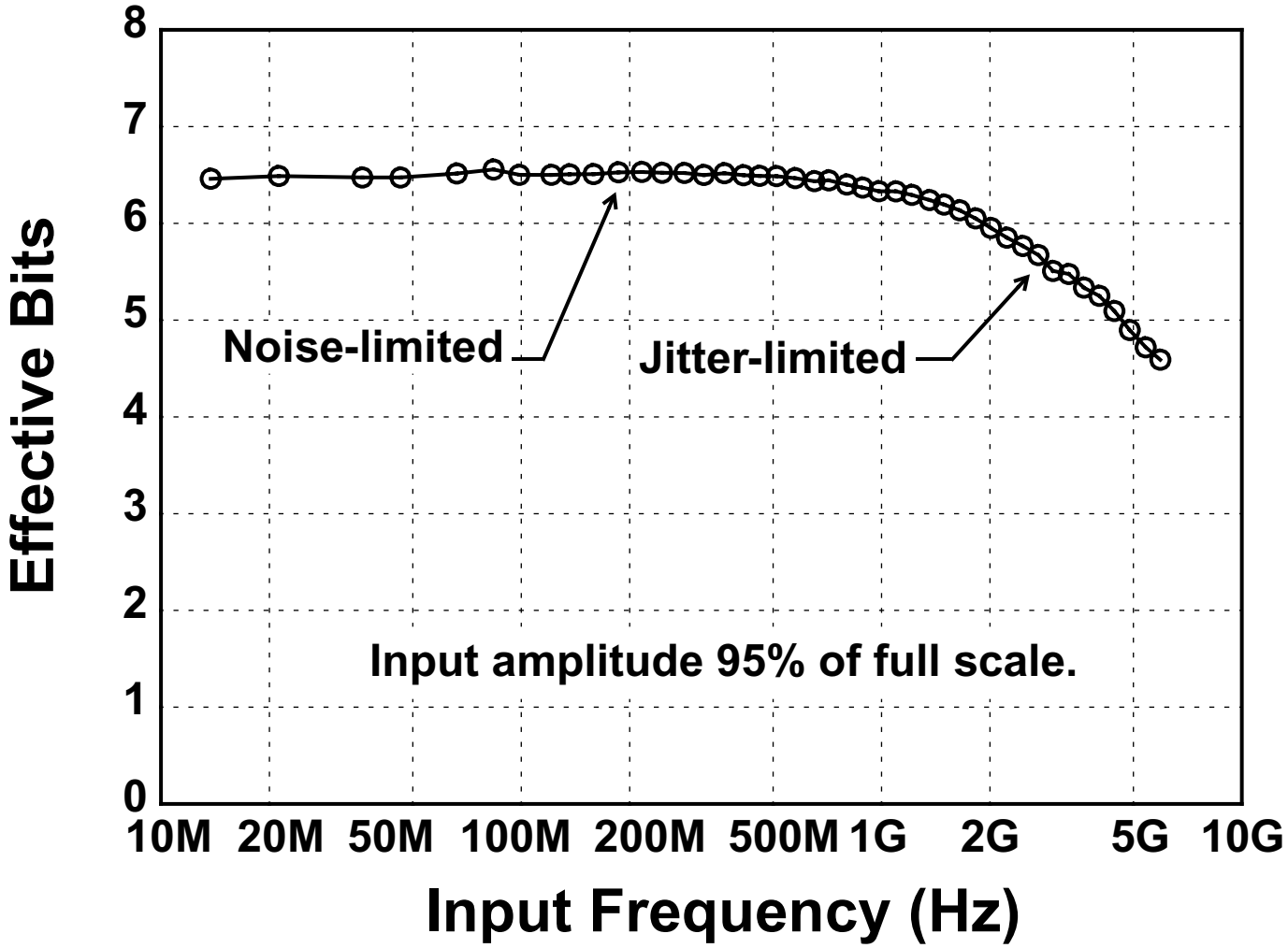


Fs = 20 GSa/s Fin = 5007.5 MHz 5.0 effective bits

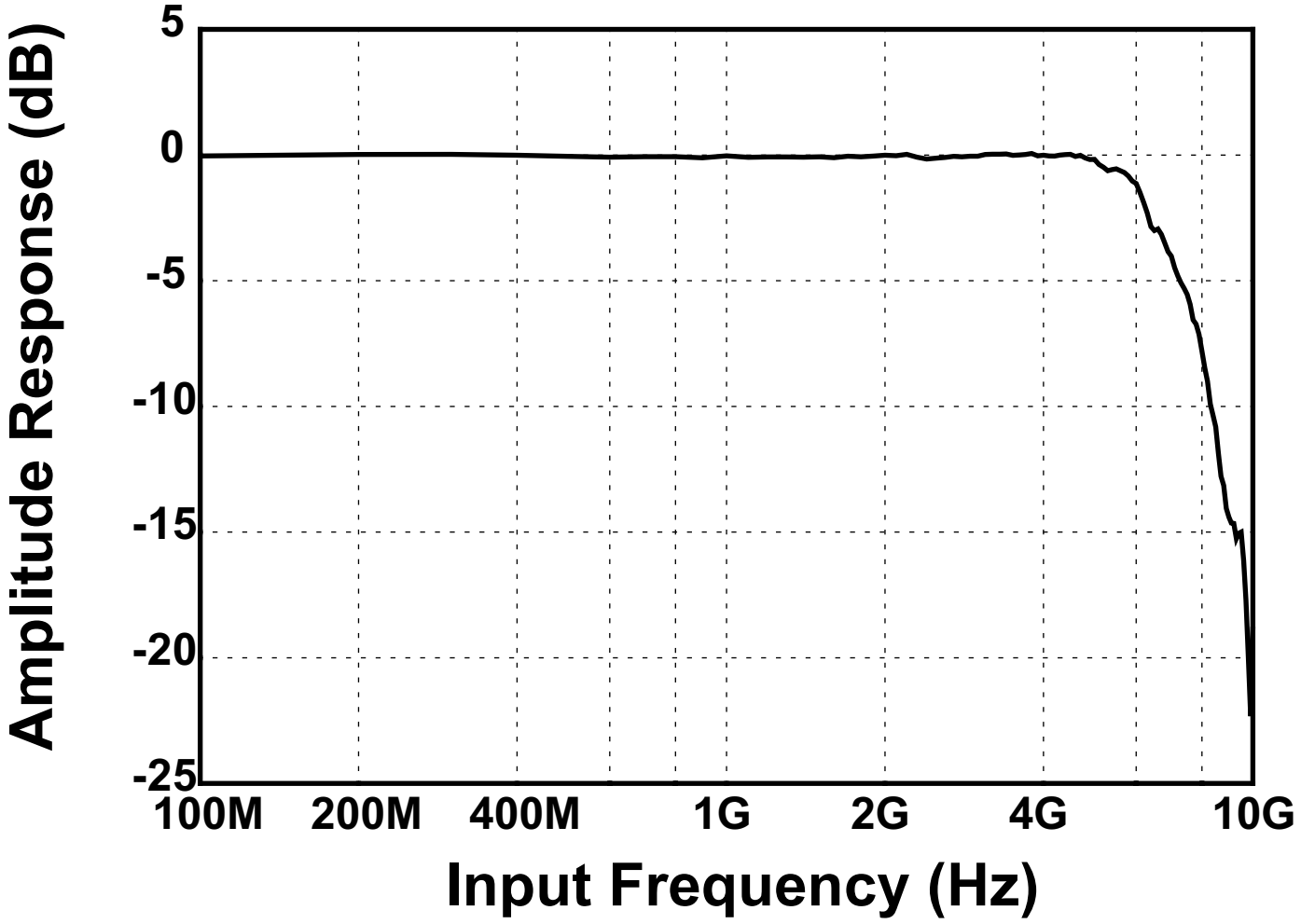
Static Linearity



ADC Effective Bits vs Input Frequency



ADC Amplitude Response

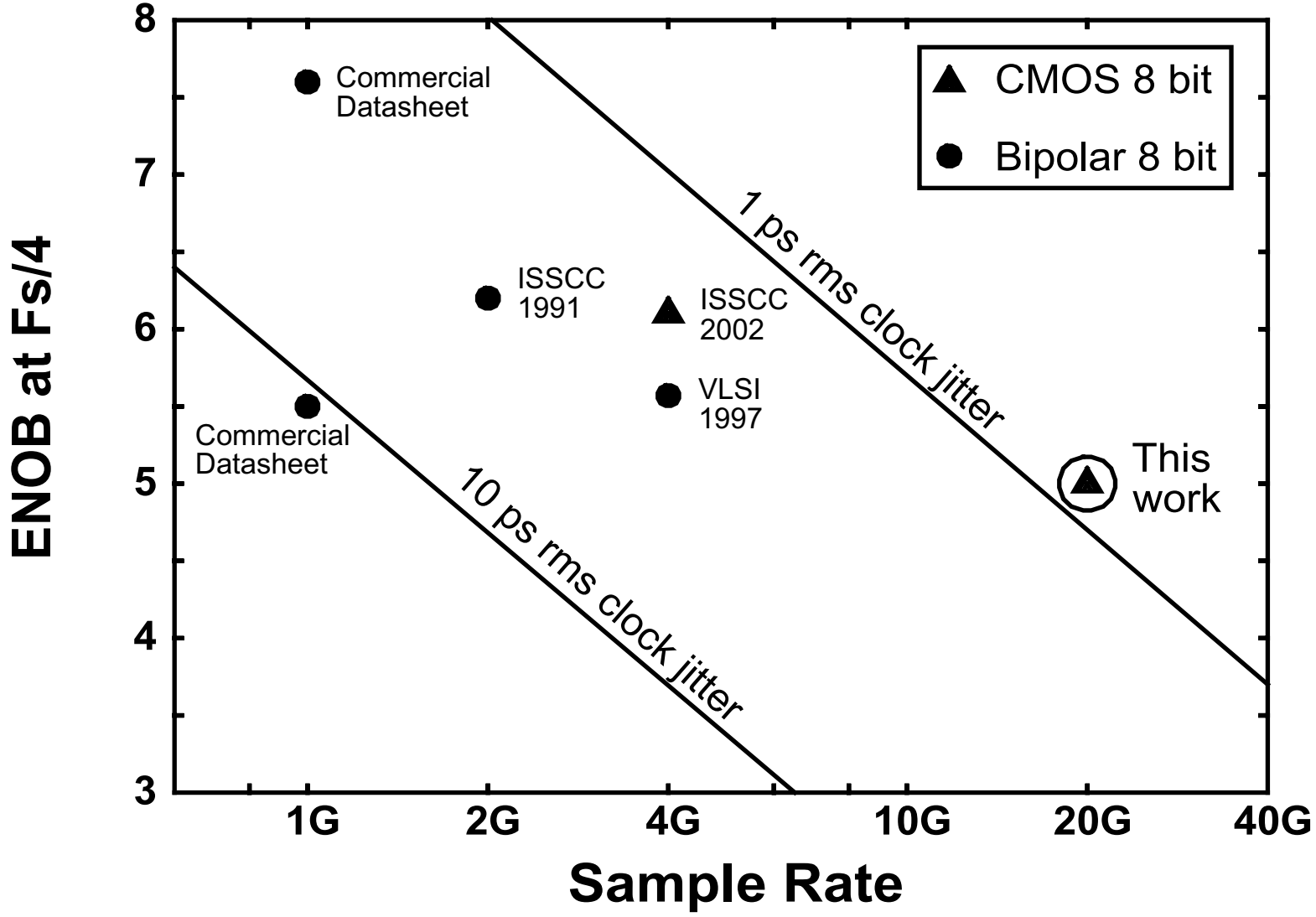


-1 dB at 5.9 GHz -3 dB at 6.6 GHz

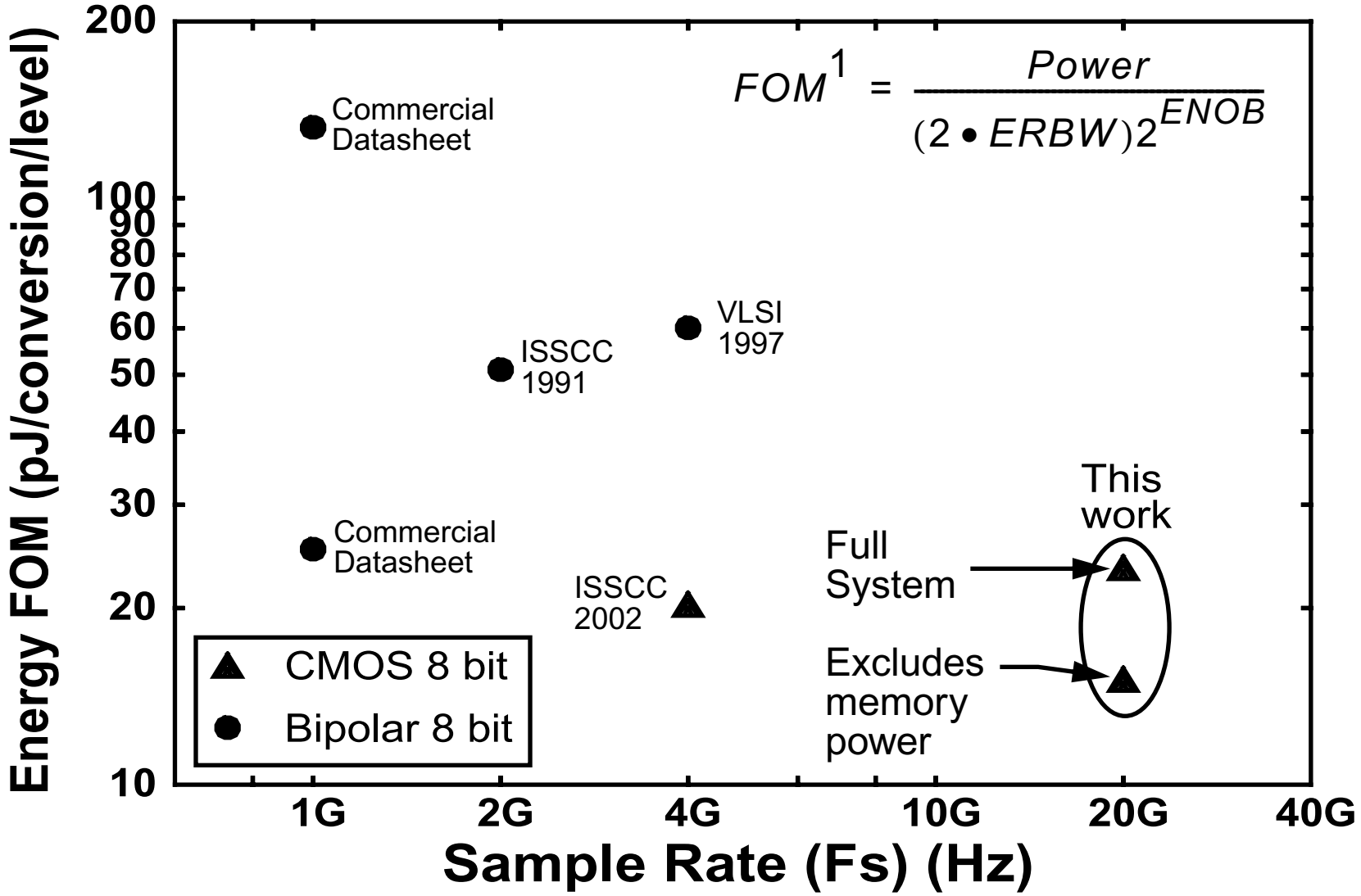
ADC Key Specs

Sample Rate	20 GSa/s	
Resolution	8 bits	
INL Intrinsic With linearity correction	 ±1.7 LSBs ±0.4 LSBs	
DNL	±0.3 LSBs	
Bandwidth	6.6 GHz	
Accuracy @ 500 MHz input @ 6 GHz input	 6.5 effective bits 4.6 effective bits	
Jitter	0.7 ps rms	
Input Range	0.25 Vpk differential	
	Buffer Chip	**ADC Chip**
Input Capacitance	0.2 pF	4 pF
Power	1 W	9 W
Chip Size	1.2 x 2.6 mm	14 x 14 mm
Technology	40-GHz SiGe BiCMOS	0.18-μm CMOS
Transistors	1000	50M
Package	438-ball BGA	

Published ADC Performance

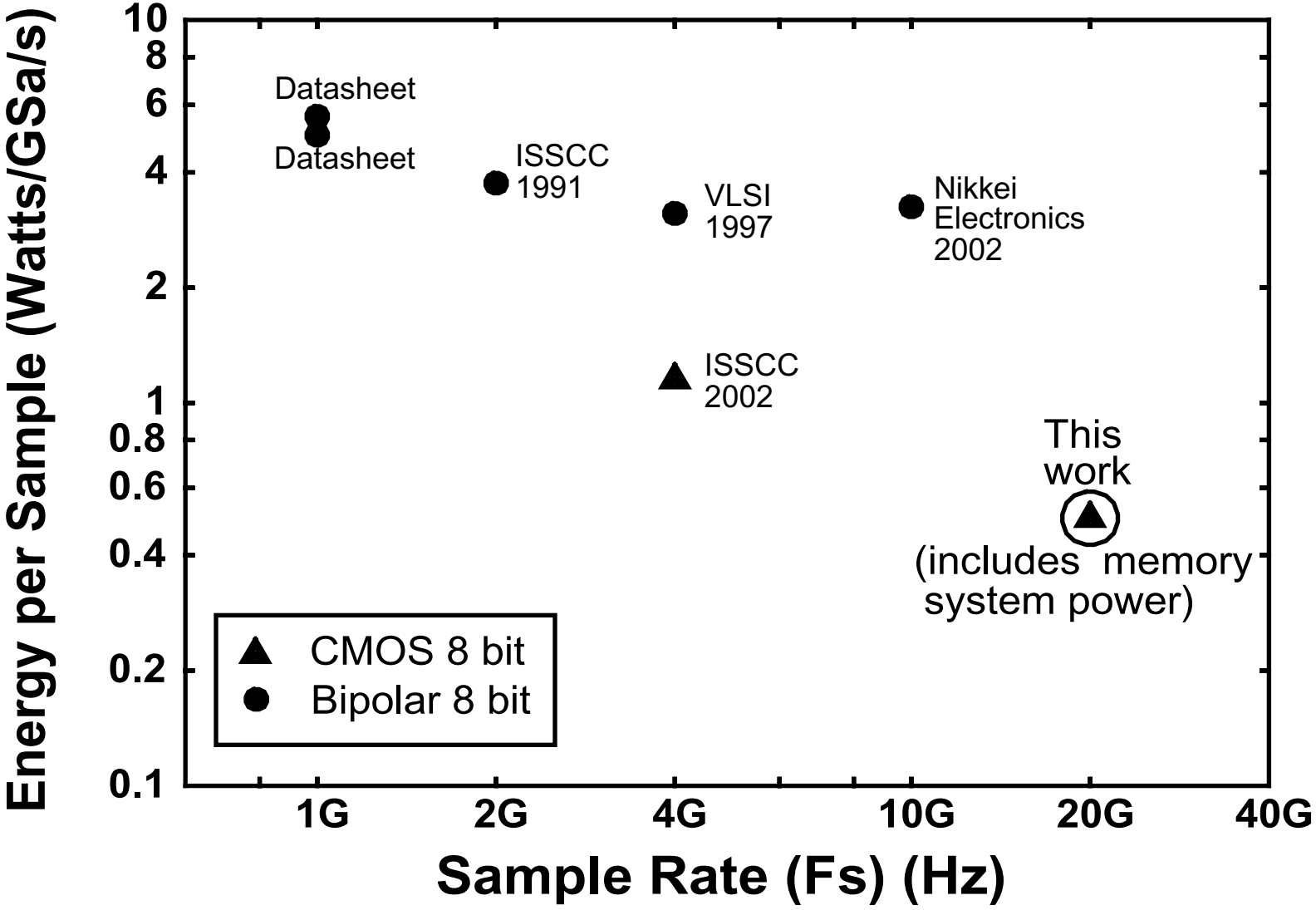


Energy per Conversion Step



[1]G. Geelen, "A 6b 1.1GSample/s CMOS A/D Converter," 2001 ISSCC Digest of Technical Papers, pp. 128-129.

Energy per Sample



Summary

Features:

- 80 interleaved ADCs with an 80-phase precision clock generator.
- SiGe buffer chip to drive the 4-pF ADC chip input.
- 1-MB on-chip memory.
- Extensive calibration to achieve accuracy.

Results:

- Sample rate 5x higher than any other CMOS ADC and 2x higher than any ADC of 6 or more bits.
- Highest reported ENOB at 5 GHz input frequency.
- Power consumption of only 500 mW per Gsample.